Journal of
Micro/Nanolithography, MEMS, and MOEMS

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Abstract. Characterization of silicon stress near copper (Cu)-filled through-silicon via(s) (TSVs) was demonstrated using high-resolution micro-Raman spectroscopy. For depth profiling of Si stress distribution near TSVs, a polychromator-based, multiwavelength excitation Raman measurement with different probing depths was used. The design concept of the polychromator-based, multiwavelength micro-Raman spectroscopy system, including the importance of the high-spectral resolution and multiwavelength excitation capability in three-dimensional (3-D) Si stress characterization, was described. Silicon stress near Cu-filled TSVs, with various sizes and layouts, was measured and analyzed before and after Cu annealing steps. Main factors impacting Si stress near Cu-filled TSVs are analyzed based on Raman characterization results on various types of TSV structures, layouts, and Cu annealing conditions. Large variations in Si stress in TSV arrays were measured in wafers with poor Cu fill characteristics and in wafers annealed in nonoptimized conditions. The Cu annealing sequence and annealing conditions are found to be significantly important for managing Si stress and the reliability of Cu-filled TSVs. Substantially lower Si stress was measured near Cu-filled TSVs with voids. Multiwavelength micro-Raman spectroscopy can be used as a very effective noncontact, nondestructive, inline TSV process and Si stress monitoring technique. [DOI: 10.1117/1.JMM.13.1.011205]

Keywords: through-silicon via; Si stress; Raman spectroscopy; inline monitoring.

Paper 13122SS received Jul. 15, 2013; revised manuscript received Dec. 20, 2013; accepted for publication Jan. 7, 2014; published online Feb. 5, 2014.

1 Introduction

Over the last few decades, the semiconductor industry has made significant improvements in chip performance and density through conventional device scaling.[1–3] Continuous device scaling in conventional ways has become more challenging as the minimum feature size approaches single-digit nanometers and with the physical limits of nanometer-scale materials used in devices with advanced designs.[3,4]

As an alternative technical pathway for vast improvements in device performance and device density using state-of-the-art device fabrication technology, three-dimensional (3-D) integration of devices through development of new packaging technologies has been actively pursued. Through-silicon via (TSV) technology has been demonstrated to deliver reduced inductance and improved device performances compared with traditional wire-bonded stacked chips.[5–7] Copper (Cu), tungsten (W), and poly silicon (Si) have been chosen as filler conducting materials depending on the final product's application and integration strategy.[5–10]

One of the main concerns in TSV technology is stress in Si induced by the difference in the coefficients of thermal expansion (CTE) between the choice of filler materials and Si during thermal cycling in the integration process steps.[5–12] The induced stress in Si near TSVs can result in electrical performance variation of stress-sensitive devices and device reliability degradation.[11–15] It can also cause catastrophic device failures such as wafer breakage, cohesive cracking in Si, and interfacial delamination between the TSVs and Si.[12,16] The estimated variation of carrier mobility of metal-semiconductor-oxide field effect transistors (MOSFETs) is higher than 7% under 100 MPa of stress in Si.[17,18] It is noted that some simulation papers show a maximum mobility change of as much as 14% in the vicinity of a TSV as a result of stress, and there are also papers that claim little or no effects on transistor I_{ON} performance with TSV stress.[14,19–22] It is not clear under what conditions (device feature size, integration, or orientation with respect to TSV) devices are affected by TSV stress. Depending on the specified tolerance for variation in transistor performance, the keep-out-zone (KOZ) surrounding the TSVs is set for the device layout design rules based on simulation results.[23,24] Understanding stress distributions near TSVs with different filler materials, liner materials, diameters, depths, pitches, and layouts is very important to set proper device layout design rules.

As Si stress characterization techniques, micro-Raman spectroscopy and synchrotron x-ray microdiffraction are used.[25–32] Micro-Raman spectroscopy is more suitable from a practical point of view. Since the probing depth of Raman spectroscopy is dependent on the excitation wavelength, choice of proper excitation wavelength is very important.[33,34] Unfortunately, most Si stress characterization reports simply

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present stress values without discussing either excitation wavelength or probing depth of the measurements. As TSVs typically have very high-aspect ratios (ARs) with depths of more than tens of micrometers, it is necessary to characterize the stress distribution three dimensionally in both planar and depth directions.[27–29] There are few Si stress characterization studies using multiwavelength micro-Raman spectroscopy, which demonstrates the presence of stress variations in the depth direction near TSVs, an important capability of 3-D stress characterizations.[27–29]

Most studies on stress-induced device performance variations near TSVs are based either on pure simulation or typical stress characterization results from a very limited, and not very well established, dataset without considering potential stress variations within wafer and wafer-to-wafer in production fabs.[23,35] More attention should be paid to practical issues in TSV process steps for better understanding of the origin of Si stress, which will lead to proper stress management and TSV process control in device manufacturing.

In this study, residual stress of Cu-filled TSVs with different dimensions and layouts fabricated on Si wafers was characterized three dimensionally using a polychromator-based, multiwavelength micro-Raman spectroscopy system. Application examples are cited of multiwavelength micro-Raman spectroscopy for process optimization and early detection of potential process-related problems through Si stress characterization. Effect of liner materials of choice, liner thickness variation, Cu fill process, and Cu annealing process on Si stress near Cu TSVs within wafer and wafer-to-wafer has been investigated. This article focuses on the effect of Cu annealing on Si stress near Cu TSVs.

2 Experiment

2.1 *Requirement of Micro-Raman Spectroscopy System for Si Stress Characterization*

Micro-Raman spectroscopy is an ideal noncontact mechanical stress characterization technique with a small measurement spot size, below 1 μm in diameter, and a submicron spatial resolution. There are a few critical requirements for a micro-Raman system for TSV-induced stress characterizations. They are measurement spot size (optical resolution or resolvability), spatial resolution (stage resolution and stage repeatability), stage travel lengths (sample size limitations), spectral resolution (Raman shift or stress resolution), measurement repeatability, measurement stability, and range of excitation wavelengths, which determine probing depths of micro-Raman measurements.[33] A micro-Raman system with spectral resolution, measurement repeatability, and measurement stability better than 0.1 cm^{-1} before curve fitting is strongly desired for resolving ~50 MPa of stress in Si near TSVs, which may result in electrical performance variations of devices.[27–29,33] The reasoning for this stringent requirement is best given with measurement examples in a later subsection.

Conventional research-grade, monochromator-based, micro-Raman systems with a focal length <1.0 m cannot meet the critical requirements of spectral resolution, measurement repeatability, and measurement stability.[29] Only one excitation wavelength can be used at a time. When the excitation wavelength is switched, tedious and time-consuming system calibration procedures must be followed.[33] Since a few mechanical moving parts are used for diffraction-grating rotation, Raman shift measurement error ± 1 cm^{-1} is not uncommon. Papers that report significant measurement uncertainty in the Raman shift (519 to 521 cm^{-1}) for stress-free Si are due to the calibration-related issues.[36,37] To meet these critical requirements, a new, long focal length micro-Raman system with no moving parts was designed.[33] For nondestructive, inline monitoring and/or characterization applications in the semiconductor industry, a fully automated, clean room compatible, micro-Raman system with 300-mm wafer characterization capability is desired. For virtual stress depth profiling, multiwavelength excitation measurement capability without system calibration between wavelength switching is also essential.[27–29,33] For inline device wafer characterization, pattern recognition and automated navigation are required.

2.2 *Polychromator-Based, Multiwavelength Micro-Raman Spectroscopy System*

To realize the desired capability of a micro-Raman system, a polychromator-based, multiwavelength, micro-Raman spectroscopy system (MRS-300) was designed and introduced.[33] The highest possible measurement resolution, accuracy, repeatability, excitation wavelength flexibility, and productivity were main foci in the design phase. Figure 1 shows the schematic illustration of the main components of the system. Details of the MRS-300 system and its semiconductor materials characterization applications can be found in previously published articles.[26–29,33] This system has been used

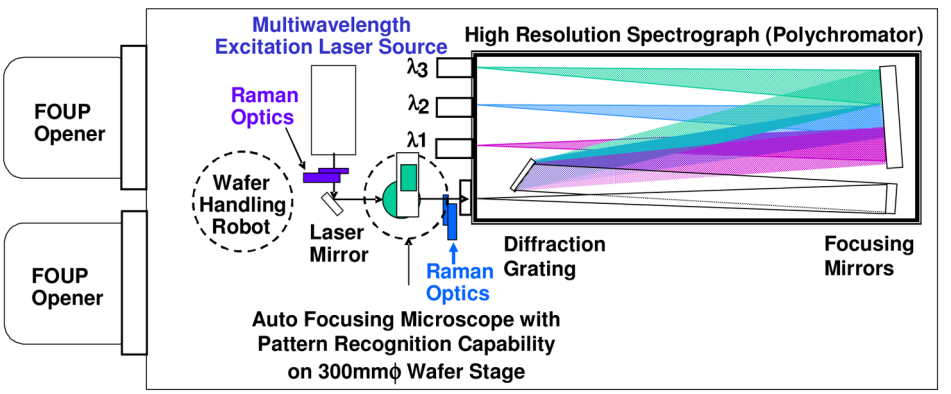

Fig. 1 Schematic illustration of a polychromator-based, high-resolution, multiwavelength micro-Raman spectroscopy system.

for characterization of stress, strain, crystallinity of Si and Si:C/Si, $Si_{1-x}Ge_x$/Si, implant damage, plasma-induced damage, dopant activation, and Si stress surrounded by Cu-filled and W-filled TSVs.[27–29,34,35,38–41]

The unique features of a very long focal length (2.0 m) focusing mirror with wide spectrum coverage, three thermoelectrically cooled charge-coupled device cameras for measuring Raman signals from three individual excitation wavelengths for virtual depth profiling, and the elimination of moving parts in the polychromator (spectrograph) allow the achievement of high-spectral resolution, accuracy, repeatability, and excitation wavelength flexibility with high productivity. Three major spectral lines (457.9, 488.0, and 514.5 nm) from a multiwavelength Ar^+-ion laser are used as the excitation source.[33] The system can also be configured for different excitation wavelength ranges of choice (e.g., ultraviolet (UV) + visible excitation wavelengths).

The as-measured wavenumber resolution exceeds 0.105 cm^{-1} in all three wavelengths (457.9, 488.0, and 514.5 nm). Since the 0.1 cm^{-1} shift of the Raman signal from Si corresponds to ~43.5 MPa, the high as-measured spectral (wavenumber) resolution and high measurement repeatability of at least ~0.1 cm^{-1} make the accurate stress analysis of Si surrounded by TSVs in this study, possibly. The MRS-300 system is equipped with pattern recognition and automated navigation capability and is capable for inline device wafer characterization.

2.3 *Raman Spectra from Stressed Si*

When a Raman signal is measured from the (100) plane of stress-free Si in the backscattering geometry, a very sharp Raman peak corresponding to the longitudinal optical phonon peak occurs near 520.3 cm^{-1}.[33] Raman peak shifts proportionally to the mechanical stress in Si at a rate of −434.5 MPa/cm.[31,36,37] To properly characterize the mechanical stress-induced carrier mobility variations within a typical mobility variability tolerance of 5% for the KOZ, a mechanical stress measurement resolution of ~50 MPa [equivalent to ~0.12 cm^{-1} in Raman shift (wavenumber) resolution] is required. The measurement repeatability of the MRS-300 system using a reference Si (100) wafer was tested for 1 year. The measurement repeatability and reproducibility of the reference Si (100) were better than 0.05 cm^{-1} (equivalent to 0.01% of 520.3 cm^{-1}). The range of Raman shift and full-width-at-half-maximum (FWHM) variations from the reference Si was smaller than 0.05 cm^{-1}. Thus, the system is capable of resolving mechanical stress in Si significantly more accurately than the minimum requirement of ~50 MPa. The major sources of Raman measurement variations were identified to be the excitation wavelength variation of the Ar^+-ion laser and a small optical axis misalignment and thermal expansion of the large polychromator due to room temperature (RT) variation (±3°C) during measurements over a long period of time. Slight systematic drift of Raman shifts was detected at specific times of the day (daytime versus night time) and was related to the air conditioner operation cycle. Operating the system in a well temperature-controlled clean room environment can significantly reduce measurement variations and improve measurement repeatability and reproducibility.

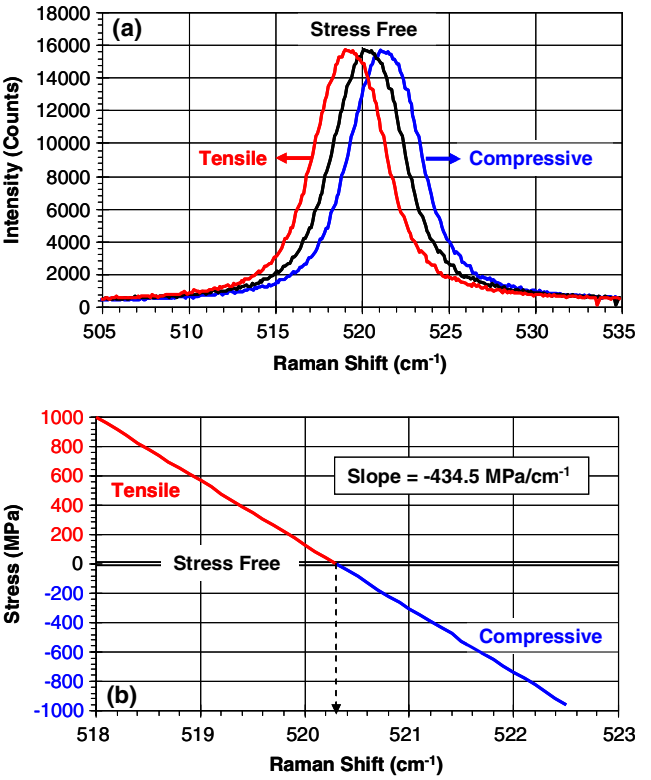

Fig. 2 (a) Typical Raman spectra measured from Si under tensile, free, and compressive stresses. (b) Relation between Si stress and measured Raman shift (peak position).

Figure 2(a) shows Raman spectra measured from stress-free and mechanically stressed Si under 457.9-nm radiation measured using MRS-300 system. For stressed characterization, controlled mechanical stress was applied to a Si wafer by bending before Raman measurements. Stress-free Si shows a sharp, symmetrical Raman peak at 520.3 cm^{-1}. The Raman peak can be fitted using a Lorentzian function. Intensity, Raman shift (peak position), and FWHM can be extracted from a Raman peak, and the values can be used for quantitative comparisons between Raman signals. Compressively stressed Si shifts the Raman peak toward the higher wavenumber side, whereas tensilely stressed Si shifts the Raman peak toward the lower wavenumber side.[33,36,37] The direction and magnitude of Si stress are extracted from measured Raman spectra in Fig. 2(b). The magnitude of Si stress is proportional to the displacement of the measured Raman peak position from the Raman peak position (520.3 cm^{-1}) of stress-free Si. The slope is equal to −434.5 MPa/cm, regardless of excitation wavelengths.[33,36,37]

2.4 *Excitation Wavelength Versus Probing Depths*

The probing depth of Raman measurement is determined by the absorption coefficient (α) of Si at the probing wavelength. The classical definition of penetration depth ($d = 1/\alpha$) cannot be used for Raman probing depth estimation, because the Raman signal (520.3 cm^{-1}) of Si is almost identical to the wavelengths of the probing laser beam, only 11.0 to 13.9 nm longer than the probing wavelengths in the range of 457.9 to 514.5 nm.[33,42] The Raman signal emanating from inside a Si crystal also attenuates in the way to free

space before collection by the objective lens of the microscope at the same rate as the probing laser beam entrant into the Si. Thus, the probing depth ($\delta = 1/2\alpha$) is typically defined by one half of the classical definition of penetration depth ($d = 1/\alpha$).[29,41] As it passes through the silicon, a Raman signal represents the weighted average of material properties from the surface to the probing depth at the probing wavelengths. Contributions from the subsurface atoms are always largest in the backscattering Raman measurement using probing wavelengths shorter than the wavelength of the absorption band edge of the material, Si in this case. Approximately 90% of the Raman signal originates from a thickness of three times the probing depth at a given probing wavelength.

Figure 3 illustrates the probing depths of three excitation wavelengths (457.9, 488.0, and 514.5 nm) from an Ar^+ laser in undoped Si. As the doping level increases, the light absorption coefficient generally increases and the probing depth becomes shallower. The figure puts the relative dimensions of TSVs and Raman probing depths in this study in perspective, with the approximate dimensions of TSVs and the device fabrication layer. By comparing intensity, shift, and FWHM of Raman peaks of Si with TSVs under different excitation wavelengths, with different probing depths, approximate depth and degree of stress and crystal imperfections can be roughly estimated. For characterizing deeper TSVs, a longer excitation wavelength with a deeper probing depth is required as the excitation light source. The benefits of multiwavelength Raman characterization of Si stress surrounded by TSVs are fairly obvious.

2.5 *Cu-Filled TSV Wafers*

As indicated in the inset of Fig. 3, Cu-filled TSVs with dimensions of 2 to 20 μm in diameter and depth ~60 μm are fabricated in 300 mm Si (100) wafers. To examine the proximity effect of Si stress near TSVs, isolated TSVs (pitch = 1:∞) with different diameters and TSV arrays, with different diameters and pitches (1:2 to 1:5), were prepared. TSVs were filled by electroplating (EP) at RT

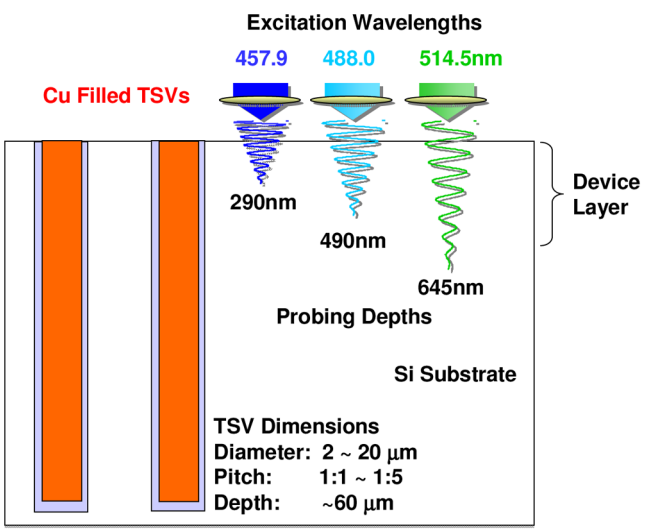

Fig. 3 Raman probing depths in Si under different excitation wavelengths. Cu-filled TSVs and device fabrication layer depth were illustrated to show the relative scale against Raman probing depths.

after oxide liner, Cu diffusion barrier, and Cu seed layer depositions.

For studying Cu annealing effects on Si stress, excess Cu layer was removed, and Cu TSVs were exposed by chemical mechanical polishing (CMP) before Cu annealing. Since the excess Cu layers on Si block the probing laser beam, the excess Cu layers must be removed and Si surface must be exposed for Raman stress characterization.

Raman measurements were performed before and after annealing to understand the evolution of Si stress along Cu TSV process steps. For Cu annealing condition optimization, Cu-filled TSVs were annealed under various conditions in the temperature range of 100 to 400°C in N_2, Ar, and forming gas ambients. The annealing was done either by a single step at a fixed temperature or a double step at two different temperatures.

3 Results and Discussions

3.1 *Si Stress Around Low-Density TSVs*

Wide pitch (1:5) (i.e., low density and nearly isolated) TSV openings with SiO_2 liners and Cu-filled TSVs, 2 to 20 μm in diameter, were prepared. Excess Cu layers were removed by CMP to expose Cu-filled TSVs and the Si surface. Raman line scan measurements were performed at the centers of the nearest TSV openings or Cu-filled TSVs, in 1 or 2 μm intervals depending on the TSV size. For 3-μm TSV openings and Cu-filled TSVs, 31 points were measured, spanning the distance of 30 μm in 1-μm interval. For 5-μm TSV openings and Cu-filled TSVs, 51 points were measured over the distance of 50 μm in 1-μm interval. For TSV openings and Cu-filled TSVs with diameter larger or equal to 10 μm, 2-μm interval Raman line scan measurements were performed. EP Cu did not completely fill TSVs with smaller diameters of 2 and 3 μm. Defects were often visible during inspection by optical microscopy. Thus, Raman characterization was done for TSV openings and Cu-filled TSVs with diameters in the range of 3 to 20 μm. Raman measurements were performed prior to Cu annealing to investigate Si stress near TSVs after Cu EP and CMP removal of excess Cu layers. The effect of Cu annealing on stress in the Si surrounded by Cu-filled TSVs, with a smaller pitch (1:2), is described in the following subsection.

Figure 4 shows the 457.9-nm excited Raman measurement results and how the Raman line scans were done. Only Raman scan results on TSV diameters of 3, 5, and 10 μm were plotted. Raman intensity was stronger in small diameter TSV openings and Cu-filled TSVs than in larger ones [Fig. 4(a)]. This is due to the significant increase of surface area per unit volume for light scattering. For small diameter (4 μm and smaller) TSV openings and Cu-filled TSVs, Raman intensity was almost equal, regardless of Cu EP. Raman intensity becomes weaker over the Cu-filled TSVs with diameter greater or equal to 5 μm. The Raman signal at the center of the Cu-filled TSVs became smaller as the diameter of the Cu-filled TSVs increased. Raman intensity was not reduced to zero, however, even at the center of the 10-μm diameter Cu-filled TSVs. This is because there are a significant number of photons from broadening of the excitation laser beam outside the effective diameter of the excitation laser beam profile. Light scattering near the Cu-filled TSVs also contributes some degree to the Raman

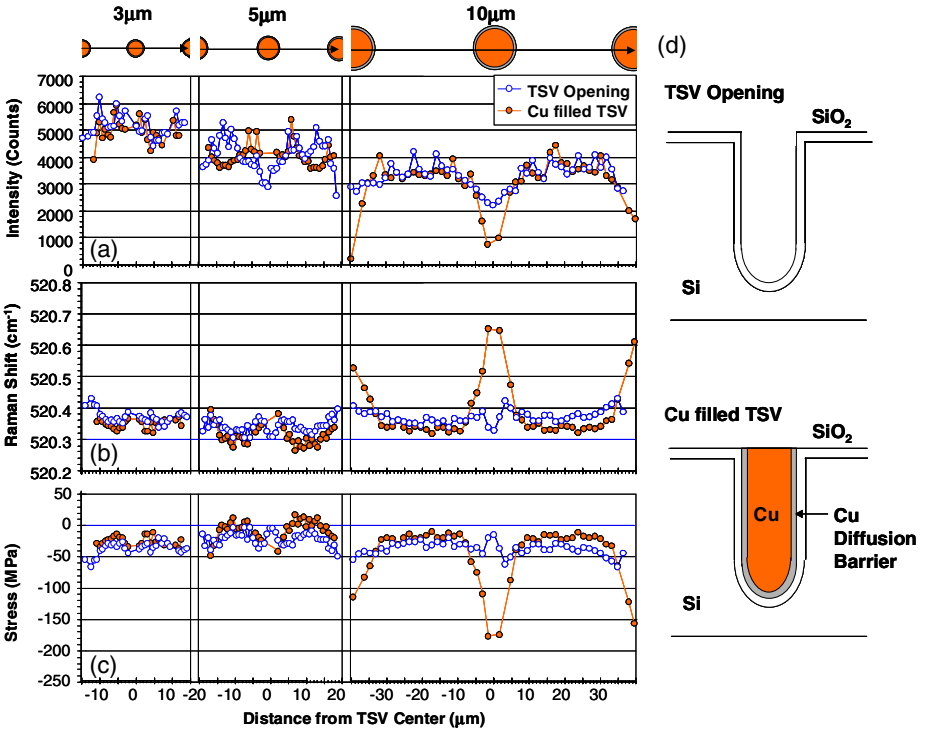

Fig. 4 (a) Raman intensity, (b) Raman shift, and (c) calculated Si stress from 457.9-nm excitation line scan measurements across nearly isolated (pitch = 1:5) TSV openings and Cu-filled TSVs with three different diameters. (d) Cross-sectional schematic illustrations of TSV opening and Cu-filled TSV used for Raman line scan measurements.

signal. When a Cu-filled TSV diameter gets significantly larger, greater than 10 μm, almost no Raman signal was detected at the center of a Cu-filled TSV. Raman peaks, from TSV diameters of 3 and 5 μm, fluctuated around 520.3 cm^{-1} (Raman peak position for stress-free Si), regardless of the presence of EP Cu in TSV openings. Raman peak shifts toward the higher wavenumber side as the measurement site approaches the Cu-filled TSV [Fig. 4(b)]. This indicates that the Raman peak position shifts toward the compressive side. The maximum Raman shift was always measured at the center of the Cu-filled TSVs, regardless of their diameter. Larger Raman shift variations were measured from the line scan, through the Cu-filled TSV with larger diameter. For 10-μm diameter TSVs, Raman shifts at the center and both ends of the line scan path (i.e., centers of TSV openings and Cu-filled TSVs) of TSV openings before Cu EP were measured to be ~520.3 cm^{-1}, nearly stress free. Raman shift at the centers of Cu-filled TSVs was consistently 0.30 to 0.35 cm^{-1}, higher than the stress-free value of 520.3 cm^{-1}. This translates to be −130 to −152 MPa in the compressive direction. This compressive stress was the effect of Cu EP to the 10-μm diameter TSV openings. Cross-sectional schematic illustrations of a TSV opening and a Cu-filled TSV help describe the effect of Cu EP on Si stress [Fig. 4(d)]. The Raman shift values were converted to Si stress values [in Fig. 4(c)]. Compressive stress variations of −20 to −170 MPa were measured over the low-density (pitch = 1:5), nearly isolated 10-μm diameter Cu-filled TSVs, prior to Cu annealing. The effect of Cu EP on Si stress on smaller diameter Cu-filled TSVs before annealing was relatively small. Since the smaller diameter TSVs with high AR are difficult to fill by EP Cu, it is difficult to separate the EP Cu integrity effect from the TSV size dependence of Si stress surrounded by Cu-filled TSVs.

The KOZ can be determined from the mechanical stress distribution measured from Raman characterization results. As the density of TSVs increases from 1:∞ (isolated TSVs) to 1:2 (TSV diameter = spacing between TSVs), higher stress values are expected between TSVs due to superposition of stress components induced by the neighboring TSVs. The determination of KOZ becomes more complex for Si wafers with different TSV structures, dimensions, layouts, and process steps.

3.2 *Si Stress Near High-Density TSVs*

Cu-filled TSV arrays with 5-μm diameter and 1:2 pitch were measured using the Raman area mapping function of the MRS-300 system. Measurement intervals in both x- and y-directions were 1 μm. Raman measurements were done before and after Cu annealing at 400°C for 10 min in N_2 to investigate the effect of annealing on Si stress. For virtual depth profiling of Si stress, multiwavelength Raman mapping was done under 457.9, 488.0, and 514.5 nm excitations. The 12 Cu-filled TSVs (3 × 4 TSVs from a large TSV matrix of the same diameter and the same pitch) were mapped.

Figure 5 shows Raman intensity contour maps [Fig. 5(a)], Raman shift contour maps [Fig. 5(b)], Si stress contour maps [Fig. 5(c)], and 3-D Si stress contour maps of the 3 × 4 TSV matrix [Fig. 5(d)] before and after annealing under 457.9, 488.0, and 514.5 nm excitations. Raman measurement was done at a measurement location by switching the excitation wavelength sequentially. Raman measurement was performed at one location at three excitation wavelengths.

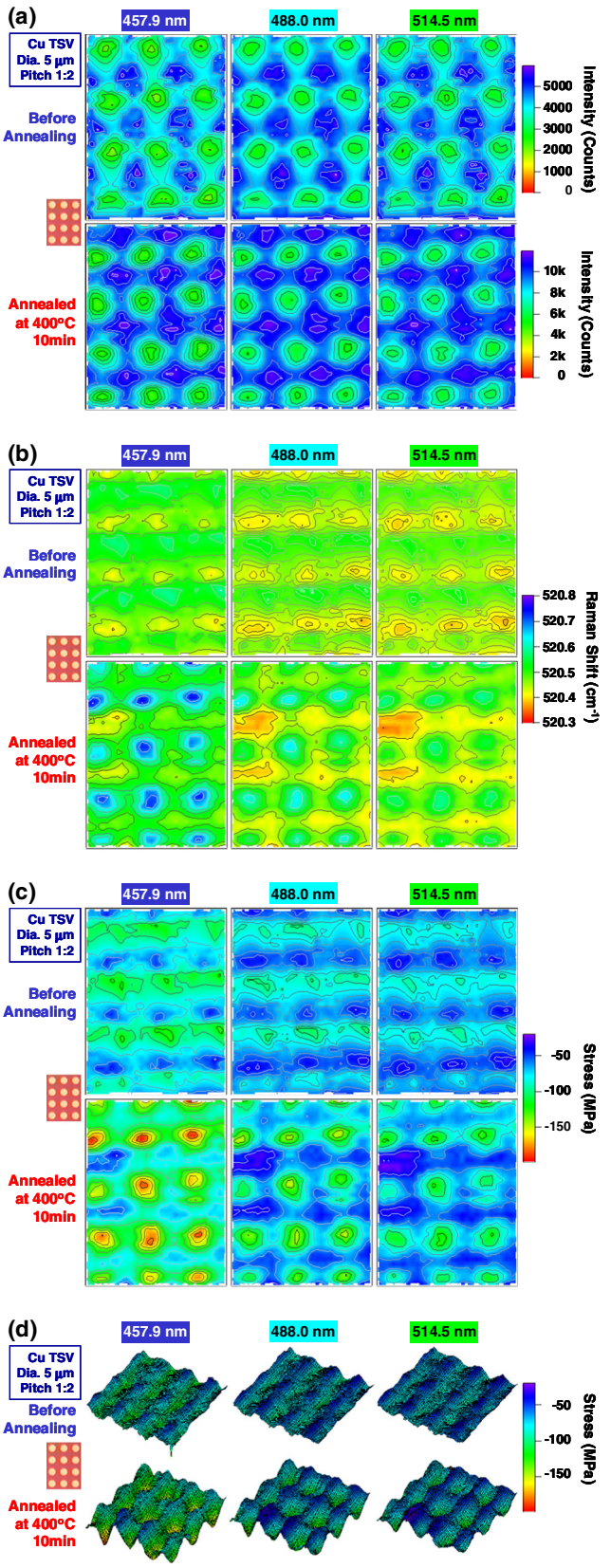

Fig. 5 (a) Raman intensity, (b) Raman shift, and (c) calculated stress maps of Cu-filled TSV arrays with 5-μm diameter and 1:2 pitch before and after Cu annealing at 400°C in N_2 under three different excitation wavelengths. (d) Three-dimensional (3-D) stress maps generated from two-dimensional (2-D) stress contour maps. Stress distribution in depth direction is clearly shown. Small microphotographs of TSV arrays are shown next to the area maps.

When Raman signal was acquired from the point under all three excitation wavelengths, measurement location was moved by 1 μm in the programmed direction. No system calibration is necessary between excitation wavelength switching due to system design, as described in the previous section.[27–29,33]

Raman intensity is significantly lower at the 12 Cu-filled TSVs [Fig 5(a)]. TSV locations can be easily identified from the Raman intensity maps. A small photograph of Raman mapping area (3×4 TSVs) is shown for reference. Raman intensity became about two times stronger after annealing, probably due to the removal of Si lattice damage caused by CMP removal of the excess Cu EP layer.

Raman shift ranges of Cu-filled TSVs under different excitation wavelengths became larger after annealing [Fig. 5(b)]. Significant changes in Raman shift ranges under different excitation wavelengths were measured from TSV arrays after annealing. They suggest the presence of stress gradients in depth direction. Since the shorter excitation wavelength Raman map shows the largest Raman shift range, we can interpret that there are large stress variations near the surface of the annealed Cu-filled TSVs and large stress gradients in the depth direction.

The stress maps show the stress variations in both planar and depth directions before and after annealing [Fig. 5(c)]. Two areas of highly compressive stress were visible from the stress maps of the annealed TSVs under all three excitation Raman measurements. 3-D stress maps make the differences easily recognizable [Fig. 5(d)]. This type of unexpected stress variation adds uncertainty in stress distribution and results in unexpected device performance variations. Understanding and controlling important process variables are the keys to optimize TSV processes for volume manufacturing.

3.3 *Si Stress Near High-Density TSVs with Different Diameters*

From the Raman characterization of isolated TSVs and high-density TSVs described in the two previous subsections, it is easy to see that the TSV diameter, TSV pitch (or layout), and annealing conditions play important roles in the resulting Si stress distribution in both lateral and depth directions.

To investigate the general trends of Si stress before and after annealing, Cu-filled TSVs with diameters ranging from 3 to 10 μm with a fixed pitch of 1:2 were characterized using the multiwavelength Raman spectroscopy system (MRS-300). Figure 6 shows the Si stress contour maps of TSVs with diameters of 4, 5, and 10 μm before and after annealing at 400°C for 10 min in N_2. Only 457.9-nm excited Raman characterization results are shown. (Note that the color scales of stress contour maps are different with TSV diameter.)

The TSVs with 4-μm diameter showed large compressive stress (−50 to −150 MPa) before annealing. The compressive stress was significantly relaxed after annealing. The stress range after annealing was in the range of 50 to −50 MPa). In contrast, TSVs with 5-μm diameter showed completely opposite trends. The stress range before annealing was in the range of −40 to −125 MPa and grew to −70 to −200 MPa after annealing. Compressive stress was added after annealing. The TSVs with 10-μm diameter started in the stress range of +30 to −230 MPa

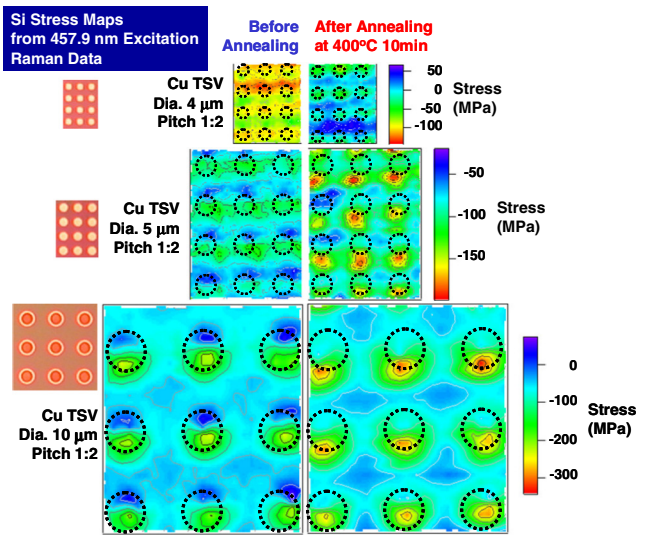

Fig. 6 Stress maps calculated from Raman measurements of Cu-filled TSV arrays with various diameters at a fixed pitch of 1:2 before and after Cu annealing at 400°C in N_2 under 457.9-nm excitation wavelength (probing depth: ~290 nm). Dotted circles in the stress maps represent TSVs. Small microphotographs of TSV arrays are shown next to the area maps.

and ended up in the range of −50 to −330 MPa. Si became more compressive after annealing. The TSVs with larger diameters tend to show higher compressive stress after annealing from the wafers investigated in this study. Since the mechanical stress in Si can result in carrier mobility variations in MOSFETs,[17,18,43] Cu-filled TSV processes such as oxide liner deposition, barrier metal deposition, Cu seed deposition, Cu EP, CMP, and annealing may need to be optimized from the stress management point of view. Stress characterization using multiwavelength Raman spectroscopy is a very effective technique to provide the necessary feedback for TSV integration process optimization.

3.4 *Inspection of Potential TSV Defects by Raman Spectroscopy*

Two wafers with 6.5-μm diameter TSV arrays were annealed with different conditions to investigate the effect of annealing conditions on TSV integrity. Annealing condition A had a single step annealing at 400°C for 10 min in N_2. Annealing condition B consists of two annealing steps at 100°C and 400°C for substantially longer times in N_2. Excess EP Cu layers of both wafers were removed by CMP after annealing.

Multiwavelength Raman measurements were done on both wafers. Figure 7 shows the 488.0-nm excitation Raman line scan measurement results across 15 TSVs over 580 μm in 1-μm interval. Optical microscopy showed identical images of the Cu-filled TSVs. TSV arrays with no visible defects were chosen for this test to demonstrate the capability of Raman spectroscopy to detect defects, which are less evident optically. The Cu TSV sizes are identical across the line scan area, while there are variations in neighboring structures. Raman intensity showed local minima at the center of Cu TSVs of both wafers [Fig. 7(a)]. Raman intensity difference between two annealed wafers under annealing conditions A and B suggests that the CMP damage

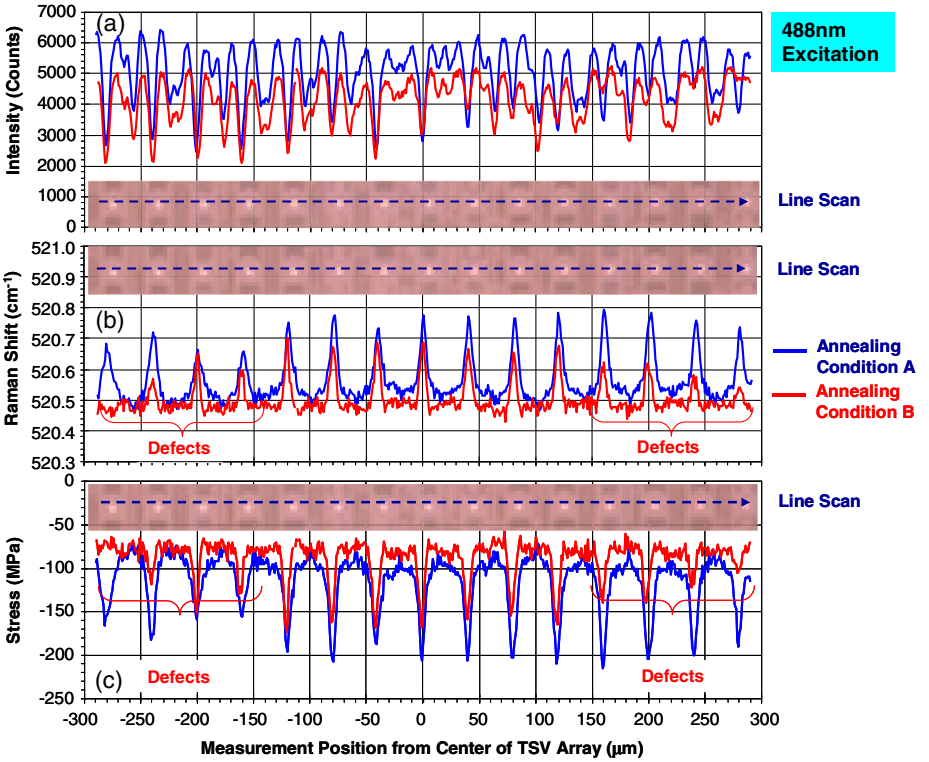

Fig. 7 Examples of 580-μm line scan results of 6.5-μm Cu-filled TSV arrays after Cu annealing under different conditions. (a) Raman intensity, (b) shift, and (c) Si stress peaks align with the centers of Cu TSVs. Annealing condition A shows significantly more consistent stress values compared with annealing condition B over the entire length (580 μm) of TSV array (excitation wavelength: 488.0 nm, probing depth: ~490 nm, and measurement interval: 1 μm).

to the Si surface was removed more efficiently by annealing condition A (Wafer A). Raman shift of line scan results on the wafer annealed under condition A (Wafer A) showed more consistent Raman shift peaks and valleys across the 15 Cu-filled TSVs. The wafers annealed under annealing condition B (Wafer B) showed irregular Raman shift peaks and valleys at both ends of the TSV arrays (labeled as "defects") suggesting large stress variations among Si regions sandwiched by Cu TSVs. The presence of Cu voids in TSVs on Wafer B must be strongly suspected from the Raman shift [Fig. 7(b)] and stress [Fig. 7(c)] line scan results.

Cross-sectional scanning electron microscopy (XSEM) has shown that the Cu TSVs near the end of TSV arrays of Wafer B have small voids and seams in the middle of the Cu TSVs. While conventional optical inspection has failed to detect potential problems in Cu-filled TSV integrity, nondestructive Raman characterization results provided useful insights into the integrity of these Cu-filled TSVs. It is possible to conclude that the Raman spectroscopy may have the ability to detect stress variation as a result of defects (such as voids and seams) in Cu-filled TSVs. By monitoring the regularity of stress distributions across the TSV arrays of interest, potential problems in Cu-filled TSVs may be detected.

3.5 *Applications of Raman Spectroscopy in 3-D Integration*

Three-dimensional integrated circuits and 3-D interconnects using TSV technology have become a very strong alternative for device performance and device density improvement, as we approach conventional scaling limits.[5–10] There have been many encouraging technical breakthroughs toward the industrial implementation of TSV technology in volume production.[5–10] Yet, we are constantly uncovering new problems and striving to find the solutions to the new challenges.[12,14,15,23,24,42,43] Understanding fundamental properties of host materials on which we are going to build and fabricate sophisticated devices is essential. There is no measurable Raman signal from metals or ultrathin dielectrics used in advanced devices. The goal of Raman measurements is to understand the material properties of Si through the frequency modulation of probing (excitation) light by Si lattice vibrations (phonons). All electronic materials used in device fabrication, whether they are directly in contact with Si or not, influence various (electrical, mechanical, etc.) properties of Si in one way or another. For Cu-filled TSVs, stress modulation of Si can cause device performance variations and has significantly adverse impacts on the potential benefits of 3-D integration.[6–8,12–15]

There are still several issues with Cu-filled TSVs. No one has complete answers to all issues and questions. Filling EP Cu in high AR trenches for TSV application was one of the many big challenges. Void-free Cu EP in TSVs became possible by optimizing EP bath composition by optimizing additives.[44] However, the thermomechanical properties of EP Cu are altered at the same time. Past understanding of EP Cu from different EP bath chemicals, with different impurities may not be useful. Thickness and properties of liner materials and Cu diffusion barriers also affect the stress of Si near TSVs. TSV dimensions and layouts strongly influence the Si stress distribution, as noticed in this study. Cu protrusion, due to the CTE mismatch between Cu and Si, is a function of thermomechanical properties of EP Cu in TSVs with different sizes and layouts. Cu annealing conditions and process integration sequences also play significant roles for successful implementation of Cu-filled TSV technology in 3-D integration.[11,27,29]

It is important to gather as much information as possible for understanding the impact of process and material variables on Si in terms of stress, residual damage, and crystallinity. Raman spectroscopy can provide the impact of process and materials on Si at measurement sites. By selecting appropriate excitation wavelengths, virtual depth profiling of Si is accomplished. By monitoring modulation and abnormal behaviors of Si properties by Raman spectroscopy, valuable insights toward process and material optimization can be gained. Early detection of potential process and material-related issues is also possible through inline monitoring, as indicated in the previous subsection.

4 Summary

Silicon stress near Cu-filled TSVs with various sizes, pitches, and layouts, with and without Cu annealing, was characterized using high-resolution micro-Raman spectroscopy. A polychromator-based, multiwavelength excitation Raman system was introduced for virtual depth profiling of Si stress distribution near TSVs. The design concept of the polychromator-based, multiwavelength micro-Raman spectroscopy system was described. The importance of the high-spectral resolution and multiwavelength excitation capability in 3-D Si stress characterization was demonstrated through virtual Si stress depth profiling.

Silicon stress near Cu-filled TSVs, with various sizes and layouts, was measured and analyzed with and without Cu annealing steps. Main factors impacting Si stress near Cu-filled TSVs are discussed based on Raman characterization results on various types of TSV structures, layouts, and Cu annealing conditions. Large variations in Si stress in TSV arrays were used to detect the potential problems in Cu fill characteristics. The source of large Si stress variations in TSV arrays was examined by XSEM imaging. Initial examination results suggested that the poor Cu fill is largely responsible for the large stress variation in the TSV arrays. The Cu annealing sequence and annealing conditions are found to have significant impact on Si stress management and reliability control of Cu-filled TSVs. Abnormal Si stress behaviors, such as unexpectedly lower local Si stress in TSV arrays, are found to be due to small voids or seams in Cu-filled TSVs. The details of XSEM imaging results on various Cu-filled TSV arrays will be reported separately. Effectiveness of multiwavelength micro-Raman spectroscopy as a very effective noncontact, nondestructive, inline TSV process and Si stress monitoring technique was demonstrated.

References

1. R. H. Dennard et al., "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid State Circuits* **9**(5), 256–268 (1974).
2. M. Bohr, "A 30 year retrospective on Dennard's MOSFET scaling paper," *IEEE SSCS Newslett.* **12**(1), 11–13 (2007).
3. K. J. Kuhn et al., "Past, present and future: SiGe and CMOS transistor scaling," *ECS Trans.* **33**(6), 3–17 (2010).
4. V. Moroz and M. Choi, "Strain scaling and modeling for FETs," *ECS Trans.* **33**(6), 21–32 (2010).

5. A. K. Stamper et al., "Through wafer via integration in CMOS and BiCMOS technologies," in *Advanced Metallization Conference (AMC)*, Vol. 2008, pp. 495–500 (2009).
6. S. J. Koester et al., "Wafer-level three-dimensional integration technology," *IBM J. Res. Dev.* **52**(6), 583–598 (2008).
7. J. Burns, "TSV-based 3D integration," Chapter 2 in *Three Dimensional System Integration—IC Stacking Process and Design*, A. Papanikolaou, D. Soudris, and R. Radojcic, Eds., pp. 13–32, Springer, New York (2011).
8. K. Johguchi, T. Hatanaka, and K. Takeuchi, "Through-silicon-via design with clustering structure and adaptive through-silicon-via control for three-dimentional solid-state-drive boost converter system," *Jpn. J. Appl. Phys.* **51**(2S), 02BE02 (2012).
9. T. Yoshinaga and N. Nomura, "Trends in R&D in TSV technology for 3D LSI packaging," Original Japanese version: published in April 2010, http://www.nistep.go.jp/achiev/ftx/eng/stfc/stt037e/qr37pdf/STTqr3702.pdf (24 February 2012).
10. M. G. Farooq and S. S. Iyer, "3D integration review," *Sci. China Inf. Sci.* **54**(5), 1012–1025 (2011).
11. U. D. Hangen, "Thermal expansion study in a TSV-structure—in-situ imaging from 23°C to 400°C in a controlled sample micro-environment," Application Note MEM06AN r1.f, HYSITRON, Minneapolis, Minnesota (20 May 2013).
12. K. H. Lu et al., "Thermal stress induced delamination of through silicon vias in 3-D interconnects," in *2010 Electronic Components and Technology Conference*, Las Vegas, Nevada, pp. 40–45, IEEE (2010).
13. M. Jung et al., "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC," in *Proc. 2011 48th IEEE/ACM International Conference on Computer-Aided Design (ICCAD'11)*, New York, pp. 317–326, IEEE (2011).
14. R. Weerasekera et al., "On the impact of through-silicon-via-induced stress on 65-nm CMOS devices," *IEEE Electron Device Lett.* **34**(1), 18–20 (2013).
15. W. Guo et al., "Impact of through silicon via induced mechanical stress on fully depleted Bulk FinFET technology," in *2012 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, California, pp. 18.4.1–18.4.4, IEEE (2012).
16. L. Xi et al., "Failure mechanisms and optimum design for electroplated copper Through-Silicon Vias (TSV)," in *Proc. 2009 59th Electronic Components and Technology Conference*, San Diego, California, pp. 624–629, IEEE (2009).
17. S. E. Thompson et al., "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices* **51**(11), 1790–1797 (2004).
18. S. E. Thompson et al., "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE Trans. Electron Devices* **53**(5), 1010–1020 (2006).
19. Y. Yang et al., "Electrical evaluation of 130-nm MOSFETs with TSV proximity in 3DSIC structure," in *IITC 2010, International Interconnect Technology Conference*, Burlingame, California, pp. 1–3, IEEE (2010).
20. E. Beyne, "3D system integration: opportunities and challenges," in Presented at the *Proc. 3-D Architect. Semicond. Integr. Packag.*, Shanghai, China (2010).
21. S. Cho et al., "Impact of TSV proximity on 45 nm CMOS devices in wafer level," in *IITC 2011, International Interconnect Technology Conference*, pp. 1–3 (2011).
22. J. West, Y. S. Choi, and C. Vartuli, "Practical implications of via-middle Cu TSV-induced stress in a 28 nm CMOS technology for wide-IO logic-memory interconnects," in *Proc. VLSI Symp. Technol. 2012*, Honolulu, Hawaii, pp. 101–102, IEEE (2012).
23. R. Borges, V. Moroz, and X. Xu, "Analysis of TSV proximity effects in planar MOSFETs and FinFETs," *Solid State Technol.* **56**(3), 16–19 (2013).
24. K. Athikulwongse et al., "Stress-driven 3D-IC placement with TSV keep-out zone and regularity study," in *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, pp. 669–674, IEEE (2010).
25. C. Okoro et al., "Extraction of the appropriate material property for realistic modeling of through-silicon-vias using μ-Raman spectroscopy," in *IITC 2008, International Interconnect Technology Conference*, Burlingame, California, pp. 16–18, IEEE (2008).
26. T. Dao et al., "Through silicon via stress characterization," in *IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 39–41 (2009).
27. A. D. Trigg et al., "Three dimensional stress mapping of silicon surrounded by copper filled through silicon vias using polychromator-based multi-wavelength micro Raman spectroscopy," *Appl. Phys. Exp.* **3**, 086601 (2010).
28. J. Gambino et al., "Stress characterization of tungsten-filled through silicon via arrays using very high resolution multi-wavelength Raman spectroscopy," *ECS Trans.* **35**(2), 105–115 (2011).
29. W. S. Kwon et al., "Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy," *Appl. Phys. Lett.* **98**, 232106 (2011).
30. C. McDonough et al., "Thermal and spatial profiling of TSV-induced stress in 3DICs," in *Proc. 2011 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, California, pp. 5D.2.1–5D.2.6, IEEE (2011).
31. I. De Wolf et al., "In-depth Raman spectroscopy analysis of various parameters affecting the mechanical stress near the surface and bulk of Cu-TSVs," in *Proc. 2012 IEEE 62nd Electronic Components and Technology Conference (ECTC)*, San Diego, California, pp. 331–337, IEEE (2009).
32. A.S. Budiman et al., "Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectron. Reliab.* **52**(3), 530–533 (2012).
33. W. S. Yoo et al., "Design of multi-wavelength micro Raman spectroscopy system and its semiconductor stress depth profiling applications," *Appl. Phys. Exp.* **2**, 116502 (2009).
34. Y. F. Tzeng et al., "Non-contact in-line monitoring of Ge content and thickness variations of epitaxial $Si_{1-x}Ge_x$ layers on Si (100) using polychromator-based multi-wavelength micro Raman spectroscopy," *Appl. Phys. Exp.* **3**, 106601 (2010).
35. Y. F. Tzeng et al., "Non-contact, in-line measurement of boron concentration from ultra thin boron-doped epitaxial $Si_{1-x}Ge_x$ layers on Si(100) by multi-wavelength micro Raman spectroscopy," *J. Mater. Res.* **26**(6), 739–744 (2011).
36. I. De Wolf, "Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits," *Semicond. Sci. Technol.* **11**, 139–154 (1996).
37. I. De Wolf, "Raman spectroscopy: about chips and stress," *Spectrosc. Eur.* **15**(2), 6–13 (2003).
38. C. W. Chang et al., "Contactless monitoring of Ge content and B concentration in $Si_{1-x}Ge_x$ epitaxial films using multiwavelength micro-Raman spectroscopy," *AIP Adv.* **2**(1), 012124 (2012).
39. C. W. Chang et al., "Micro-Raman characterization of Ge diffusion and Si stress change in thin epitaxial $Si_{1-x}Ge_x$ layers on Si(100) after rapid thermal annealing," *J. Mater. Res.* **27**(9), 1314–1323 (2012).
40. C. W. Chang et al., "Multiwavelength Micro-raman characterization of epitaxial $Si_{1-x}Ge_x$ layers on Si(100) and in-line process monitoring applications," *J. Electron. Mater.* **41**(11), 3125 (2012).
41. W. S. Yoo et al., "Characterization of strain-engineered Si:C epitaxial layers on Si substrates," *ECS Trans.* **45**(6), 23–29 (2012).
42. W. S. Yoo et al., "Non-contact and non-destructive characterization alternatives of ultra-shallow implanted silicon PN junctions by multi-wavelength Raman and photoluminescence spectroscopy," *J. Electrochem. Soc.* **158**(1), H80–H84 (2011).
43. T. Kinoshita et al., "Thermal stresses of through silicon vias and si chips in three dimensional system in package," *J. Electron. Packag.* **134**, 020903 (2012).
44. C. Okoro et al., "Impact of the electrodeposition chemistry used for TSV filling on the microstructural and thermo-mechanical response of Cu," *J. Mater. Sci.* **46**(11), 3868–3882 (2011).

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