

Low-cost coincidence counting apparatus for quantum optics investigations

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ABSTRACT

We have recently started investigating quantum optics for our advanced laboratory and quantum mechanics classes. For a small department, the expenses of much of the apparatus is daunting. As such, we look for places where we can reduce the costs while still providing benefits for our students. One of the places where there can be some cost savings are in the coincidence counter. The coincidence counter is a critical piece of the investigation, and while not the most expensive component, cost savings are still available. We have developed a low-cost coincidence counter (less than \$50) based on a Cypress Programmable System on a Chip (PSoC). The PSoC is quite flexible. It has a microcontroller as well as FPGA like capabilities which enable us to build the coincidence detection and the counter. The design process and several investigations will be presented.

1. INTRODUCTION

Quantum Optics experiments have become very popular investigations in physics teaching laboratories. A rich body of investigations has been developed such as the Grainger experiment, Single Photon interference and the Quantum Eraser to name a few [1-5]. These experiments allow students to learn about optics, interferometry, the fundamental nature of light, single photon detection, counting methods and quantum mechanics. In the course of working with single photon experiments, our students learn about different techniques for aligning optics and fiber optics as well as the fundamental optics. The increased interest in the single photon laboratories is, in part, the availability of lower cost Single Photon Avalanche Diode detectors (still quite expensive), lower cost coincidence detection, much more affordable laser systems (less than \$100) and affordable down conversion crystals (BBO, ~\$500).

There have been a number of different coincidence detectors developed of varying degrees of simplicity and cost. Notable are the several designs described in Branning et. al. [6, 7] which have involved both discrete logic elements and an FPGA with a cost of \$300 or a more depending on how you do the configuration. Refs[8, 9] presents designs solely based on an FPGA with time stamp features and a cost of approximately \$100. Ref [10] has several other designs.

Part of the process for us to learn about single photons is to develop our own apparatus. The focus of the present work is to describe the development of a lower cost and simpler coincidence detection system. Our design goals were to develop a relatively straightforward and simple system that required very little assembly but would be capable. What we came up with has quad inputs and six counters that are each capable of collecting up to four-fold coincidences and involves very little hardware work. Ultimately, our system costs approximately \$40. It is based on a Cypress PSoC 5 microcontroller prototyping kit CY8CKIT-059.

2. WHAT IS A PSoC?

PSoC stands for Programmable System on a Chip. The PSoC 5 is a mixed signal microcontroller system. It comes with a 32 bit ARM Cortex M3 processor, a variety of analog components such as operational amplifiers, comparators, a 20 bit analog to digital converter, two 12 bit analog to digital converters, four digital to analog converters, a 24 bit digital filter system and 24 universal digital blocks (UDB). The UDB's consist of a matrix of uncommitted Programmable Logic Devices (PLD's) and a digital interconnect. The PLD may be configured to be any number of digital devices from simple logic elements to more complex digital devices such as counters, pulse width modulators and communication. Another interesting feature of the PSoC is that almost every pin is reconfigurable for analog or digital. Furthermore, Individual

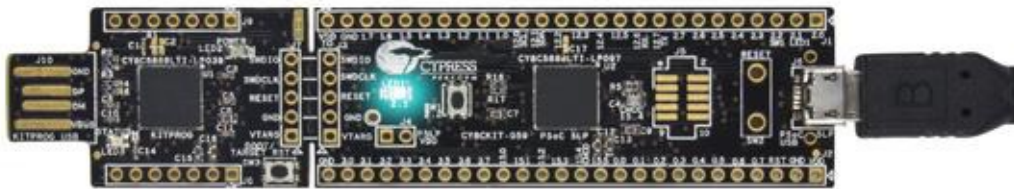


Figure 2. Photograph of the Cypress CY8CKIT-059 prototyping kit used in this project. Image from <http://www.cypress.com/?rid=108038>

Programming the PSoC involves using free and downloadable, but proprietary integrated development system from Cypress (for windows only)- PSoC Creator [X]. PSoC Creator allows you to graphically design the digital and analog components of the PSoC with drop and drag components (counters, PWM's, OpAmps, A/D converters, Capacitive sensors, etc.) and a wiring tool. Coding is completed in the environment using "c".

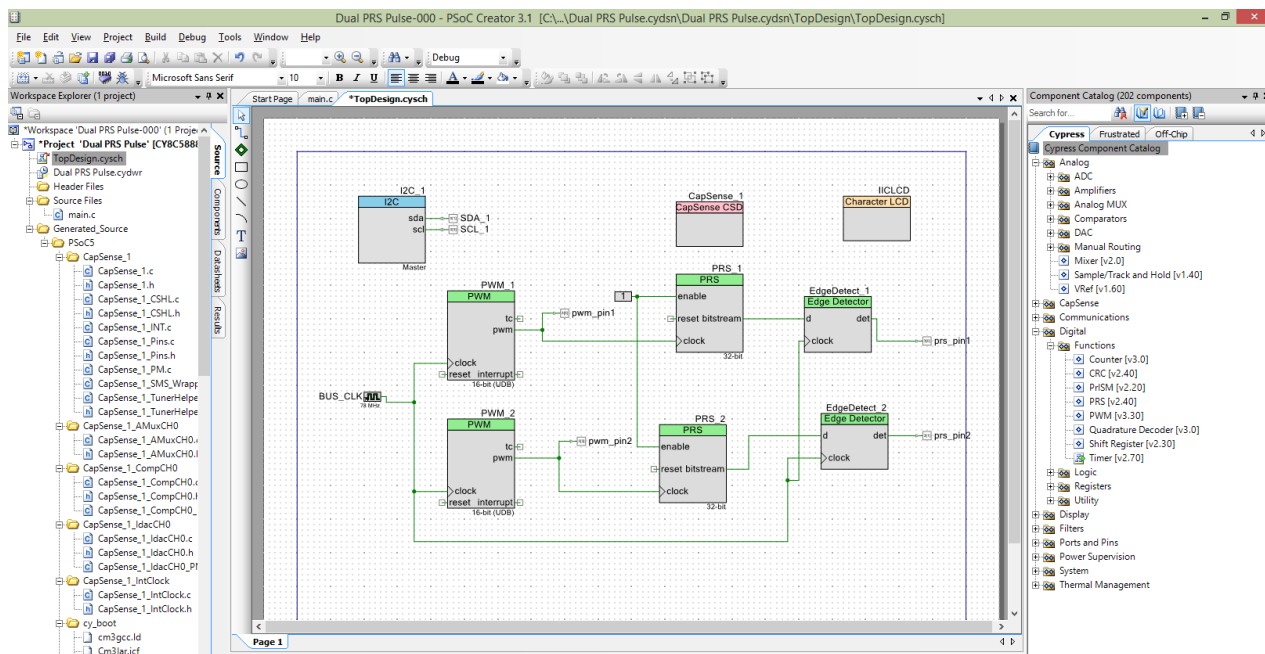
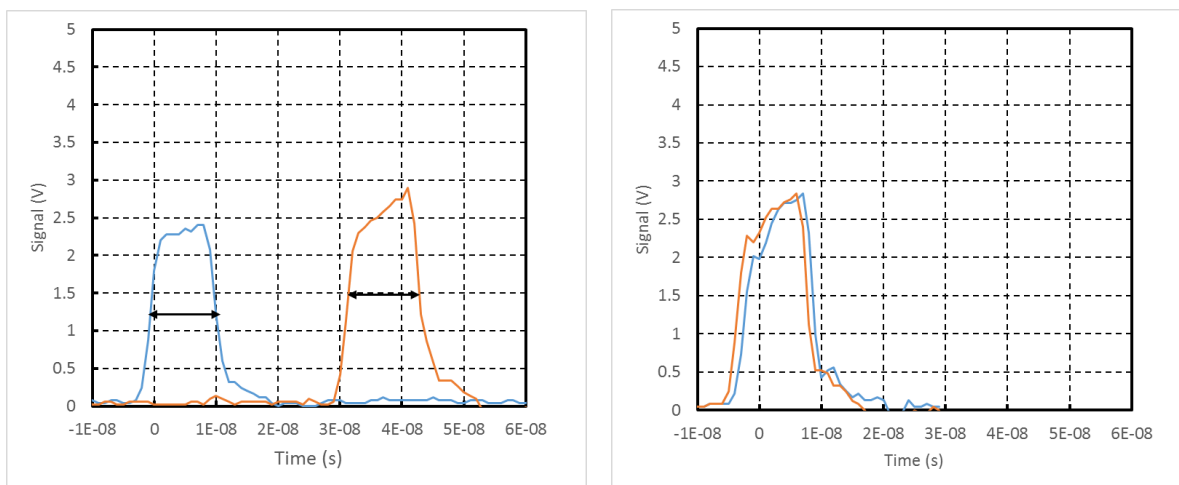


Figure 3. Image of PSoC creator showing the design board for our Pseudo Random Pulse generator used later in testing.

3. PSoC 5 COUNTER

The counter and coincidence detector that we developed has four, 50 ohm terminated input channels, six 24 bit counters, an adjustable window (0.1 s to 10s at present) and six outputs. The coincidence detection is programmable via capacitive buttons allowing any combination of inputs from single channels to four-fold coincidences to be counted. After each coincidence detection, the pulses are synchronized to the clock for counting. Each of the coincidence detectors also pass the pulses to each of six outputs which allow the counters to be combined to allow a greater number of inputs.

The coincidence detection is determined by the circuit shown in Figure 4. It consists of four OR gates to choose the inputs and an AND gate does the coincidence detection. The Control register is the interface between the processor and its firmware and the digital circuitry. If one of the control register bits is set high as one of the inputs for an OR gate, then the output of the OR gate will always be high and therefore that input will not matter. Our tests of the OR and AND gates indicate that they are very fast with very short propagation times (we measured differences in propagation times of less than 1 ns for 5 AND gates and 4 NOT gates). The largest propagation delays come from the input and output buffers. This is on the order of 35 ns (See Figure 3).



Similar to the design in Ref [9], we did not include pulse shaping into our system in part because our detectors generate 10 ns pulses and we felt that it was not necessary. However, this is something we can revisit at a later time.

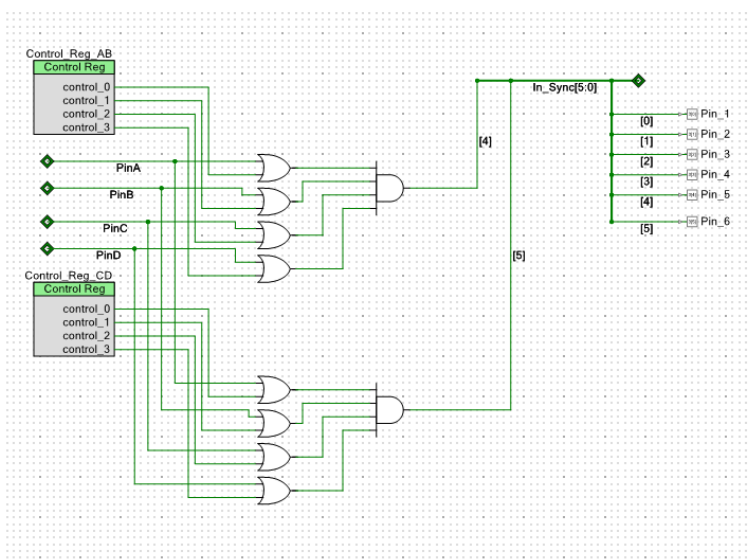


Figure 4. Section of the PSoC Counter showing the channel selection and coincidence detection circuitry. Control registers allow the CPU to interact with logic circuits through firmware. PinA – PinD are the inputs. Pin_1 – Pin_6 are the outputs. In_Sync[5:0] is a bus.

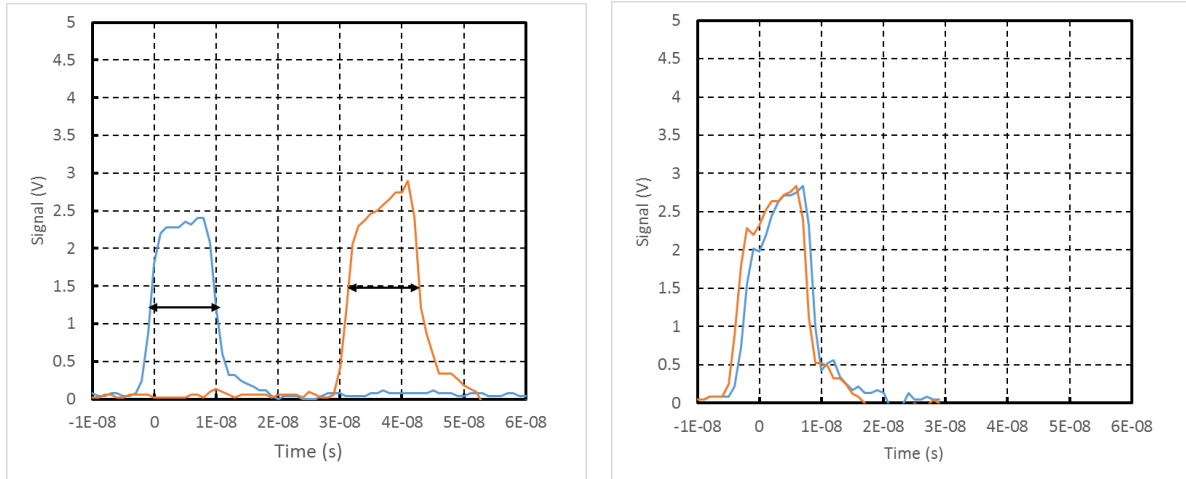


Figure 5. The graph on the left shows the propagation time for the input (signal on the left, blue) to the output (signal on the right, orange). The delay is approximately 35 ns. The graph on the right compares the input – then straight through the IC to the output (orange) with the input being directed through 5 AND gates and 4 NOT. The delay is approximately 1 ns.

We were able to use the counter by mounting the prototyping kit on an electronic breadboard. However, to make connections more secure we designed a simple two sided circuit board which was etched in the laboratory. The circuit board is shown in Figures 6A and 6B. The development kit plugs into this board. The board has the termination, and the BNC connectors for input and output. The board also has capacitive buttons for controls. It also mounts the LCD screen which provides feedback for the selection of what to count as well as showing the counts of the first four counters. It would also have been very simple and cheaper to assemble the entire counter on a perf-board. The cost of the entire counter is given in Table 1.

Table 1. Table of costs for assembling the counter.

Item	Cost	Vendor
CY8CKIT-059 PSoC5 prototyping kit	\$10.00	http://cypress.com
4x20 serial LCD	\$8.00	http://ebay.com
Double sided circuit board material	\$6.99	http://circuitspecialists.com
BNC connectors (10)	\$12.70	http://mouser.com
51 Ω Termination Resistors (4)	\$0.40	http://mouser.com
Total	\$38.09	

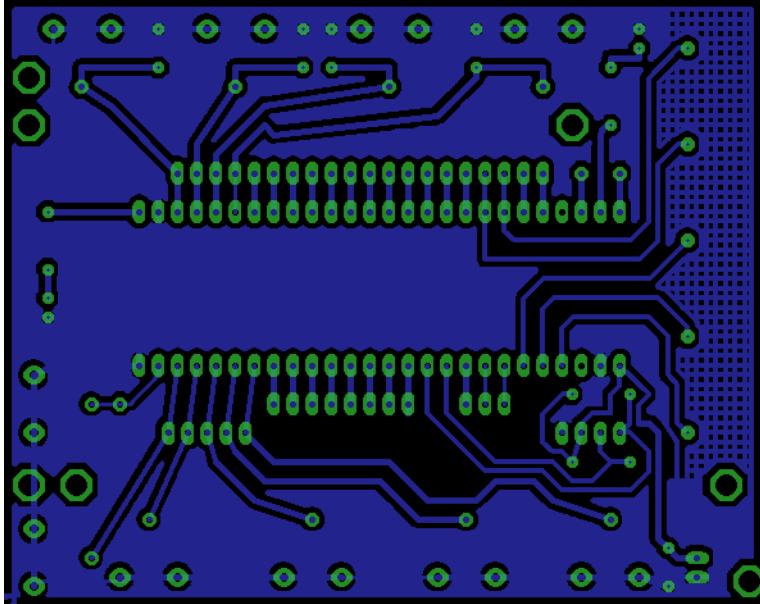


Figure 6A. Bottom layer of the circuit board for the PSoC Counter. Artwork is shown 1:1

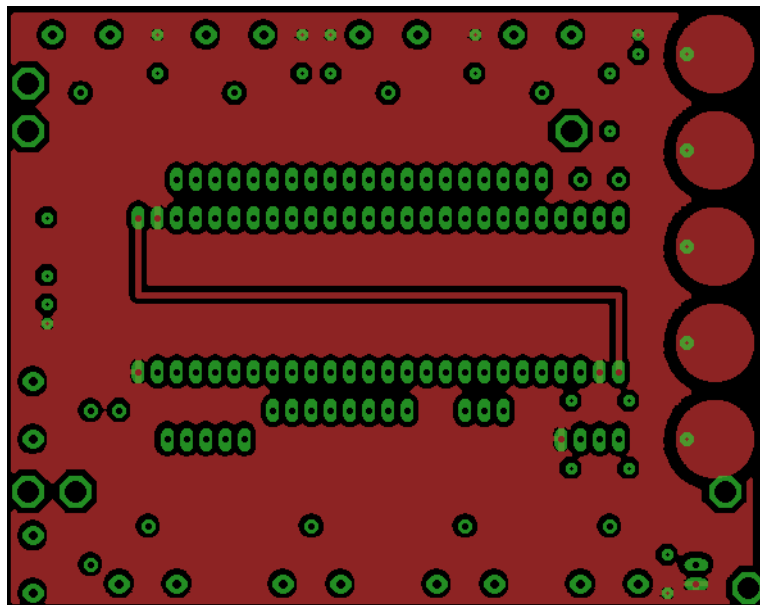


Figure 6B. Top layer of the circuit board for the PSoC Counter. Artwork is shown 1:1

Choosing what combination of input channels will be counted is set using capacitive buttons which are etched on the circuit board as shown in Figure 6B and Figure 7B. The capacitive buttons have the advantage of being fairly easy to interface directly to the microcontroller and have no moving parts. All of the counts can be sent through the serial connection to the computer. We found when using our SPAD's that the output is below TTL thresholds. We set the PSoC input to be LVTTL, which is functional. However, as a future alternative, we will actually set the input voltage level on the prototyping kit using VDDIO.

The finished counter prototype is shown in Figure 7. All files, PSoC Creator files, Eagle Cad circuit board files, and interface software are available at Ref [13].

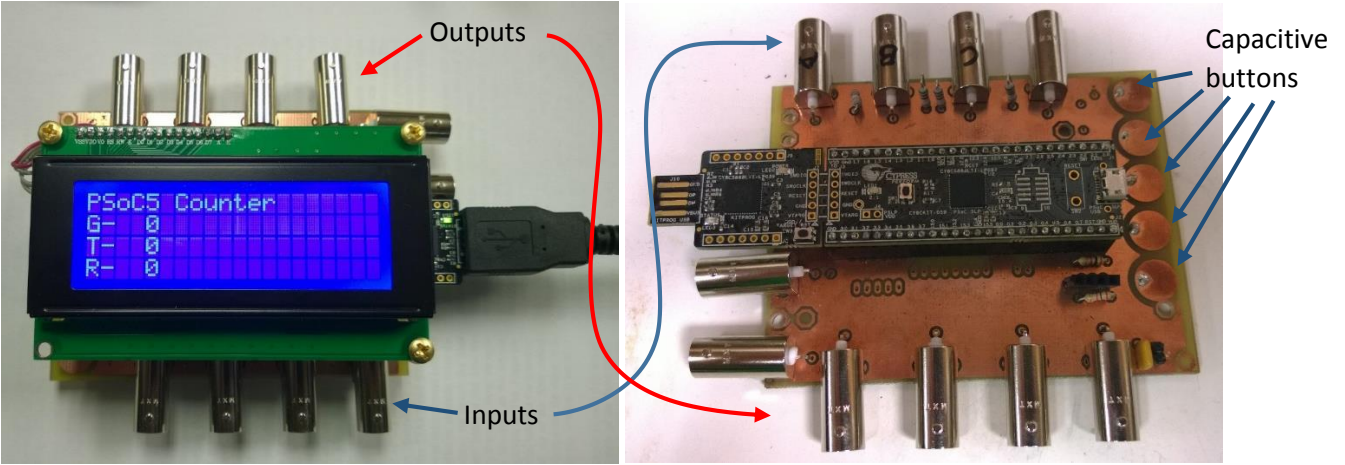


Figure 7. On the left, the completed counter system. On the right, we see the circuit board. The capacitive buttons are on the right hand side. The inputs are at the top. And the six outputs are on the bottom of the image. .

4. COUNTER AND COINCIDENCE TESTS.

To test the counter we initially used a pulse generator which allowed us to use pulses of 5 ns or longer. We used a 50MHz counter to compare the PSoC counter with measured counts. A 200 MHz oscilloscope was used to examine the pulses in and out of the PSoC counter. Figure 8 shows the counts for 10 ns pulses using the PSoC counter vs. the counts measured using the 50MHz counter as a function of input frequency. Exceeding 25 MHz, the PSoC counter is unable to keep up and starts to miss counts making it inaccurate. We do not consider it usable for more than 20MHz. We also found that for pulses shorter than 10 ns, the counter would also miss counts. Therefore, the limitations we place on the device are a minimum pulse length of 10 ns and a maximum count rate of 2×10^7 cps. Since we are using 24 bit counters, the window needs to be adjusted to match the count rate since the maximum counters for the 24 bit counter is 2^{24} counts or 1.678×10^7 counts. For low count rates we can use longer windows.

As a preliminary test of the counter, we assembled a dual channel pseudo random sequence (PRS) generator on a second PSoC 5 prototyping kit so that we could examine the response of the system using random inputs. As in Ref 2 and 6, the coincidences in two random events has been shown to follow the form of $C = \tau \times R_1 R_2$, where C is the number of coincidences and R_1 is the counts on channel 1 and R_2 is the counts on channel 2. τ is the detection window. The data is shown in Figure 9 and yields a detection window of approximately 21.5 ns which is consistent with the pulse duration from our PRS.

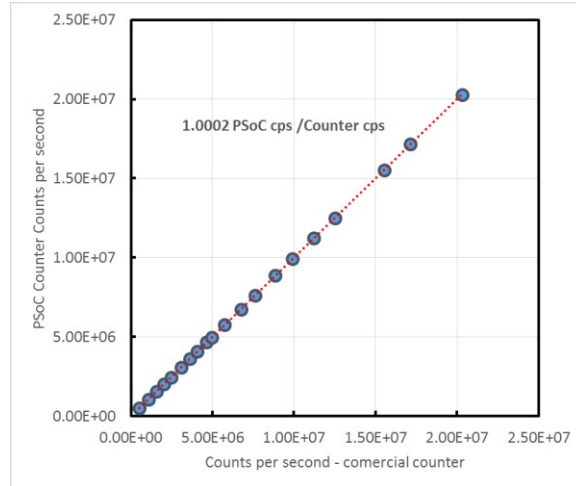


Figure 8. PSoC 5 Counter response vs. Commercial Counter. This indicates the counter is fairly well calibrated.

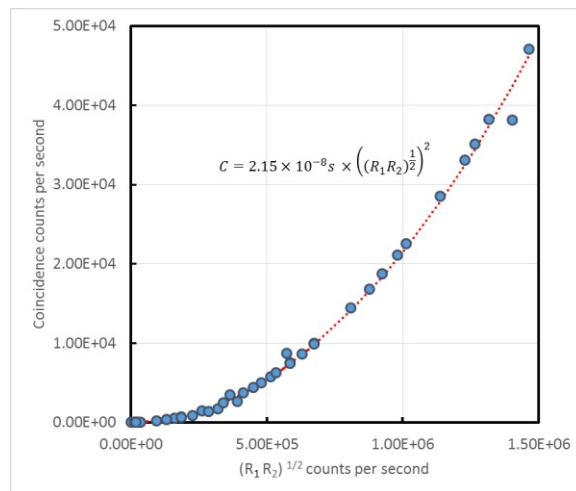


Figure 9. PSoC 5 Counter response to the two channel PRS. Analysis of this data indicates that the pulses generated by the PRS generator were approximately 21.5 ns since we do not make use of pulse shaping on the PSoC.

5. EXPERIMENTAL TESTS

As a final test of this counter, we put it into our single photon system. Since this is our first foray into quantum optics we are showing several simple tests as presented in Ref 2. Our experimental system is similar to the one described by Mark Beck [14] with fiber coupled detectors and RG 780 filters in the path to protect the detectors.

In experiment 1, we use a small incandescent bulb (a random process) with ND filters and look at random coincidences between two detectors which allows us to determine the coincidence window. For the random thermal process we would expect the anticorrelation coefficient, $\alpha^{2d} = \frac{R_{AB}}{R_A R_B \tau}$ to be 1 (just as it was for the pseudo random pulse generator). In this expression, R_{AB} is the number of coincident counts per unit time, R_A and R_B are the counts per unit time of each of the detectors, and τ is the coincidence window. The 2d superscript indicates we are using two detectors as shown in Figure 10.

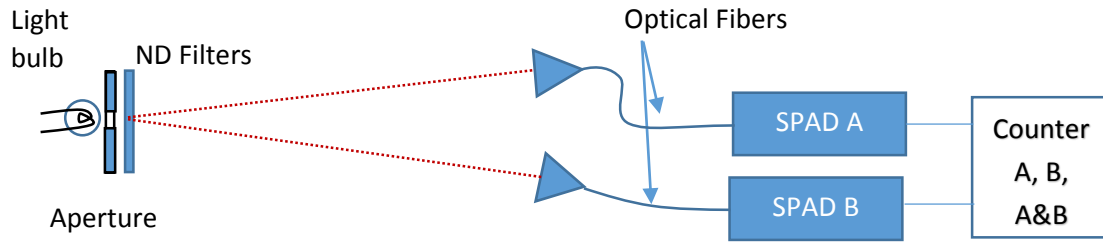


Figure 10. Setup with an incandescent light bulb to measure the coincidence window width which was 10.5 ns, in agreement with the pulse width from our SPAD's.

Finally, we performed a dual channel investigation using the nominally single photon source from a down conversion system. The experimental set up is shown in Figure 11. We would hope to measure the anti-correlation coefficient with a value much greater than 1. However, to date we have only measured it to be 1.2, which is only two standard deviations above 1 and is rather disappointing. We currently attribute this failing to the pump laser which has a horrible beam shape (doughnut) and are in the process of replacing it with a different system.

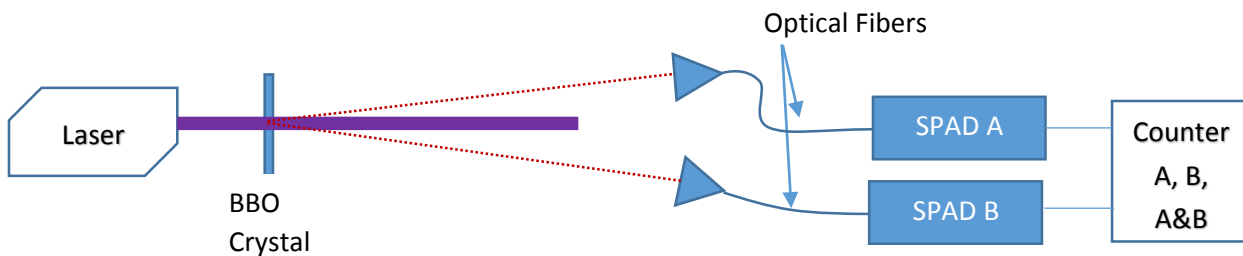


Figure 11. Setup for single photon generation using spontaneous down conversion

6. CONCLUSIONS

We have demonstrated a fairly simple counter which can be assembled for approximately \$40. Tests indicate that it is functional. While it presently is limited to four-fold detections, we have the ability to expand the number of inputs and outputs. What we cannot do is expand the number of counters without decreasing counter resolution to 16 bit. This would then greatly reduce the counting windows.

There are improvements to be made to the system. A different circuit board design would place the capacitive buttons on the bottom of the circuit board and use the board as the lid to a box rather than an open frame system. It would also be helpful to utilize the onboard USB port rather than use the programmer for data communication. Data communication could be improved by better support software with graphical display – either through LabView or with a custom Python program. We also would like to add an SD card reader so that data can be stored directly on an SD card without the need for a computer.

At present we make little use of the processor on the microcontroller other than to read the counters, display the counts and then to send those to the computer. With a little effort we can have it collect statistics and report these.

Finally, we are considering developing our own circuit board, rather than depend on the prototyping kit because there are some advantages such as the ability to control the input levels of different ports. This would still be a one chip solution, however, the complexity of such a system would be quite a bit higher, requiring a more complex custom circuit board.

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- [14] Beck, M., <<http://people.whitman.edu/~beckmk/QM/>>