# Lithography Alternatives meet Design Style Reality; How do they "Line" Up?

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## ABSTRACT

Optical lithography resolution scaling has stalled, giving innovative alternatives a window of opportunity. One important factor that impacts these lithographic approaches is the transition in design style from 2D to 1D for advanced CMOS logic. Just as the transition from 3D circuits to 2D fabrication 50 years ago created an opportunity for a new breed of electronics companies, the transition today presents exciting and challenging time for lithographers.

Today, we are looking at a range of non-optical lithography processes. Those considered here can be broadly categorized:

- Self-aligned lithography
- Self-assembled lithography
- Deposition lithography
- Nano-imprint lithography
- Pixelated e-beam lithography
- Shot-based e-beam lithography

Do any of these alternatives benefit from or take advantage of 1D layout? Yes, for example SAPD + CL (Self Aligned Pitch Division combined with Complementary Lithography). This is a widely adopted process for CMOS nodes at 22nm and below.

Can there be additional design / process co-optimization? In spite of the simple-looking nature of 1D layout, the placement of "cut" in the lines and "holes" for interlayer connections can be tuned for a given process capability. Examples of such optimization have been presented at this conference, typically showing a reduction of at least one in the number of cut or hole patterns needed.[1,2]

Can any of the alternatives complement each other or optical lithography? Yes.[3] For example, DSA (Directed Self Assembly) combines optical lithography with self-assembly. CEBL (Complementary e-Beam Lithography) combines optical lithography with SAPD for lines with shot-based e-beam lithography for cuts and holes.

Does one (shrinking) size fit all? No, that's why we have many alternatives. For example NIL (Nano-imprint Lithography) has been introduced for NAND Flash patterning where the (trending lower) defectivity is acceptable for the product. Deposition lithography has been introduced in 3D NAND Flash to set the channel length of select and memory transistors.

**Keywords:** Low $k_1$, 1D design style, gridded design rules, pitch division, lines and cuts, design source mask optimization (DSMO), self-aligned pitch division, DSA, CEBL

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## 1. DESIGN HISTORY

Modern electronics began in the early twentieth century with the invention of the vacuum tube. An active component which exhibited gain opened the door for countless circuits performing amplification, oscillation, Boolean logic functions, memory functions, sensory functions, and more. All of these circuits shared one characteristic: they were built from discrete three-dimensional (3D) objects. Circuits were constructed one component at a time, with interconnecting wires soldered to terminals and positioned either in air or later printed wiring boards (PWB).

Eventually, as circuit complexity increased, the 3D approach ran into familiar limits: the component density was limited by scaling of vacuum tubes and discrete transistors, and the interconnect density was limited by yield and reliability (*e.g.* cold solder joints). Transistors and PWB's helped, but power density became a new limiter.

The invention of the integrated circuit and the planar process for fabrication changed electronic design completely. The circuit designer had to not only create a circuit topology as a schematic diagram, but in addition had to translate the circuit into a physical layout composed of layers of planar elements. The two-dimensional (2D) planar elements were just polygons which had to be drawn in the right shape and with the right relationship to other polygons.

The transition from 3D design to 2D design was painful, and some designers could not relate to the new style. Fortunately, they could still design systems using IC's so 3D component-based design didn't go away.

Planar processing relies on the significant advantage of uniformity in thin film deposition and etching. This "subtractive" approach permitted much tighter tolerances in the component and interconnect parameters as well as giving better matching between critical components.

An implicit assumption in planar processing is that the design layout, transmitted through an optical mask, is faithfully replicated in each layer as they are built up during the process flow. This was an excellent assumption for many years as the resolution of optical exposure tools kept pace with the requirements of each design.

However, as cost-driven scaling resulted in smaller and smaller features, optical patterning became more and more challenging. The familiar Rayleigh equation (half-pitch = $k_1$ $\lambda$/NA) suggested scaling through reduced wavelength, increased numerical aperture, or reduced manufacturing margin. Twenty years ago, illumination sources transitioned from mercury lamps at 435nm and 365nm to deep ultraviolet excimer lasers at 248nm and 193nm. Larger and more complex lenses featured larger numerical apertures until 0.93 was reached.

The fitting factor $k_1$ in the Rayleigh equation has been decreasing for recent technology nodes. For $k_1$ values below ~0.6, resolution enhancement techniques (RET) such as optical proximity correction (OPC), off-axis illumination (OAI), and phase shift masks (PSM) have been introduced to maintain reasonable pattern fidelity.

The use of RET was accompanied by a rapid increase in the number of design rules. More and more rules were restricting how shapes were drawn, and placing more constraints on the allowed relationships between shapes. These rules were hard to follow, difficult to check against, and often still allowed "hot spots" or regions with necking or bridging.

An alternative approach was presented at SPIE Advanced Lithography in 2008.[3] Logic designs created from one-dimensional (1D) "line" patterns were shown. The design information was contained in the breaks or "cuts" in the lines. SAPD was also demonstrated for line pitch scaling.

The 1D design style using "lines" and "cuts" was shown to achieve good circuit density and permit layouts without hotspots. Figure 1a shows an example of a 2D layout of a logic inverter. Figure 1b shows an example of a 1D layout for the same logic function. Note that the number of horizontal metal tracks and the number of vertical poly tracks are the same in both cells; hence, the cell areas are the same even though the 1D style is more lithography friendly.

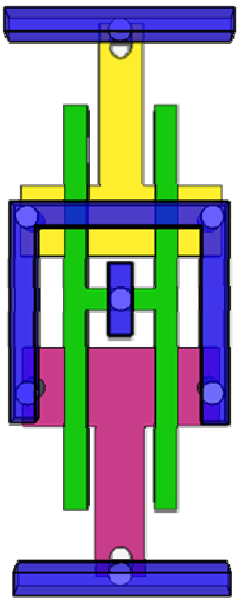
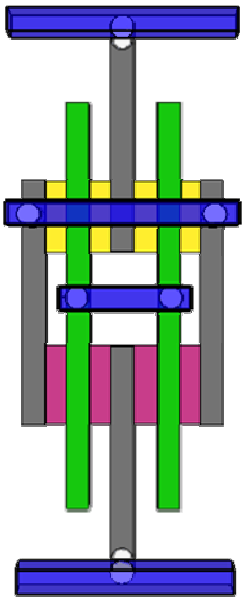


**Figure 1a. 2D style layout of logic inverter.**



**b. 1D style layout of logic inverter.**

Just as highly uniform thin films were important for the move from 3D to 2D circuits, highly uniform lines are important for the transition from 2D to 1D circuit layouts. The uniformity of the line CD, small LER, and significant improvement in CDU after etch or CMP gives the designer better components to work with. This reduces design time and improves simulation versus silicon correlation.

## 2. ALTERNATIVE LITHOGRAPHY

Even for the 1D design style, 193i optical lithography is limited to a pitch of ~80nm. However, as shown in Figure 2, metal-1 pitches are below 80nm from the 22nm node onwards. Self-aligned pitch division (SAPD) is the preferred approach to scale lines and is currently in high volume production.[5,6] The cut and hole layers require multiple patterning at 16nm and below, with the transition occurring at different nodes for different design layers.[7-15] Cut and hole multiple patterning has been simplified by reducing the mask count with design co-optimization and reducing the mask complexity with OPC-Lite.

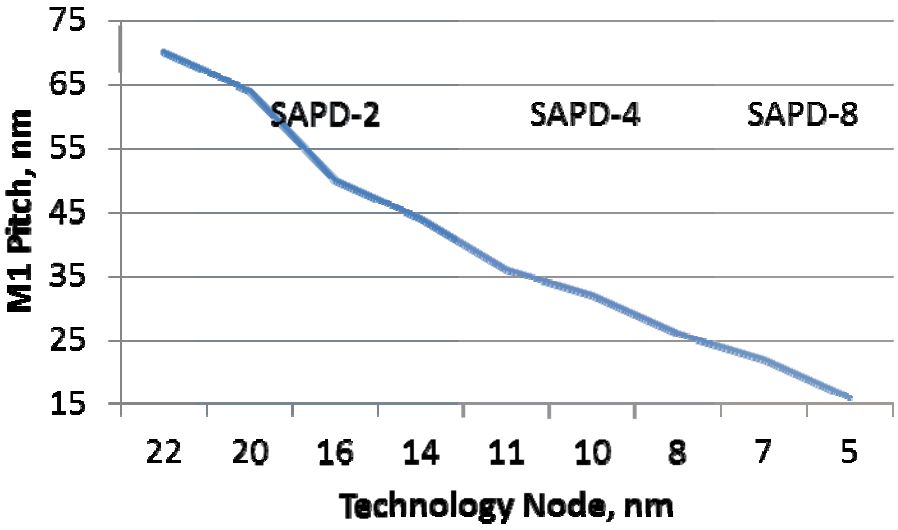



**Figure 2. Metal-1 pitch for sub-22nm logic technology nodes.**

SAPD is one example of an alternative lithography technology. Other alternatives include:

- Self-aligned lithography, such as spacer-defined pitch division by 2, 4, or more. This technology has been in production in NAND Flash memories for 4 generations, and in logic technologies for 1-2 generations. Tokyo Electron has demonstrated line patterns down to 5.5nm half-pitch.[]
- Self-assembled lithography, such as directed self-assembly (DSA) is being widely researched. The Ideal program at Leti is an example of intensive work on the materials, unit processes, and process module.
- Deposition lithography, such as the row and select lines in 3D NAND Flash, is in high volume production as the number of active layers increases to 48 and beyond.
- Nano-imprint lithography, used today for products such as NAND Flash at Toshiba, has a steadily improving defectivity and is available from Canon.
- Pixelated e-beam lithography, such as from Mapper used in the Leti Imagine program.
- Shot-based e-beam lithography, such as the Multibeam Corp. CEBL writer.

Ironically, even though several of these technologies are in high volume production, they are labeled as “alternative.” A more appropriate description may be “complementary.”[4]

Equally interesting is the comparison of the use of these alternatives versus conventional optical exposure tools. In products such as 3D NAND Flash, the number of alternative lithography steps may be equal or exceed the number of optical lithography steps. For example, the memory array stack may have 48 layers of select and row lines. Since the thickness of the poly layer sets the “L” of the storage transistor, each of those deposition steps is also a lithography step. The “stair-step” formation in these memory chips starts with an optical patterning step for one layer, then multiple self-aligned steps for subsequent layers; the ratio of self-aligned-to-optical layers is set by etch selectivity and is steadily increasing.[16]

## 3. 1D DESIGN STYLE IMPACT ON LITHOGRAPHY

Of the alternative lithography technologies previously listed, several are well suited to take advantage of the 1D layout style. Others, such as nano-imprint and pixel-writing e-beam, may be better suited for other applications.

SAPD is widely used for the line pattern in 1D layouts. Pitch division by two is suitable for the 14-16nm nodes, and is in high volume production. Pitch division by four has been demonstrated on production equipment and is expected to be used for the 10nm node. Pitch division by six or eight has been successfully done with today's production equipment for capability demonstration. Line edge roughness of less than one nanometer has been shown. CDU of ~1% has also been reported.

DSA is being developed for both line patterns as well as hole patterns. Extensive work has been done to evaluate defectivity caused by materials and structures. For example, material "pitch" versus template spacing has some combinations with good pattern fidelity and some with high defectivity.[17,18]

Hole shrink is important to get sub-20nm holes using any patterned lithography approach. Optical lithography can get to ~60nm holes and needs a shrink process. E-beam and EUV have a limit of about 20nm because of stochastic effects due to the small number of photons/electrons needed. DSA and low temperature deposition processes (*i.e.* "edamame" by TEL) can shrink hole dimensions with good uniformity.[19]

The shot-based multiple-column CEBL technology is well suited for patterning the cuts and hole in a 1D layout.[20,21] The concept takes advantage of the low pattern density in these layers to overcome the traditional low throughput of pixel-based e-beam direct write tools. Additional capabilities not available in mask-based lithography are expected to be useful in the IOT era.

Additional process extensions for 1D layouts are anticipated.[22] For example, the local interconnect line layer could be self-aligned to the gate layer; cuts would be done in a conventional manner. A "layer-to-layer" self-aligning process could be applied to hole layers based on DSA or self-aligned deposition; in either case, unlike today, the self-aligning material may need to remain on the wafer.

## 4. CONCLUSIONS

The 1D layout style has allowed IC scaling using production-proven manufacturing tools to dimensions far beyond what was thought possible with optical lithography. Alternative technologies have proven cost effective and will continue to be used to complement optical lithography. On-going process and tool development is expected to further leverage the advantages of 1D layouts. Other trends such as 3D structures in NAND Flash will continue to benefit from alternative lithography technologies.

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