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RESEARCH PAPER

In situ electrical property quantification of memory devices by modulated electron microscopy

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ABSTRACT. E-beam inspection based on voltage-contrast (VC) defect metrology has been widely utilized for failure mode analysis of memory devices. Variation in e-beam image contrast indicates shorts, opens, and void defect inline inspection in the idle of production line. Meanwhile, accurate measurement of threshold voltage and the source–drain current is required to characterize memory cell through multilayers. However, in the subthreshold region of memory cell, VC is weakened due to gate voltage stimulated by electron dose of e-beam scanning. We developed a modulated beam imaging with the SEM vector scan system to enhance VC contrast and defect inspection capability. Reliability of the modulated electron microscopy is validated by comparing with physical probing test result for process variation of Boron doping and annealing conditions in full wafer processing. VC with the modulated electron microscopy is well correlated to the probing test result. Image contrast of the modulated microscopy can differentiate contact via on floating circuit and disconnected floating circuit. We applied the modulated electron microscopy for inline electrical defect detection at the middle of manufacturing line of integrated circuits. The defect distribution map by the modulated electron microscopy was confirmed to reproduce the physical probe test result. By achieving inline electrical characterization before back end of line, yield loss issues can be detected and characterized 2 weeks earlier than conventional method. Moreover, this ability to detect and characterize memory cell issues inline is supposed to contribute to overcome the yield learning cycle bottleneck.

Keywords: modulated electron microscopy; voltage contrast; electrical failures; 3D NAND; floating circuit; e-beam inspection

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1 Introduction

1.1 3D NAND Memory

Authors 3D NAND memory stacks memory cells vertically and uses a charge trap flash architecture as shown in Fig. 1. The vertical layers allow larger areal bit densities without requiring smaller individual cells. 3D NAND was first announced by Toshiba in 2007.[1,2]

An individual memory cell is made up of one planar polysilicon layer containing a hole filled by multiple concentric vertical cylinders. The hole's polysilicon surface acts as the gate electrode. The outermost silicon dioxide cylinder acts as the gate dielectric, enclosing a silicon nitride

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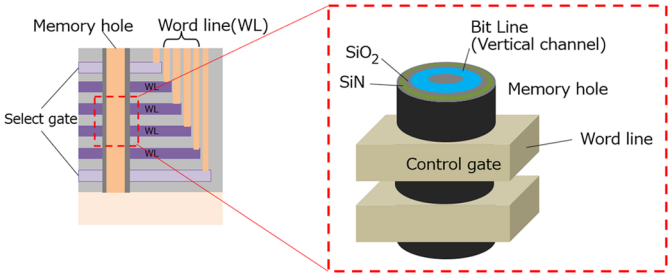

Fig. 1 Memory cell of 3D NAND.

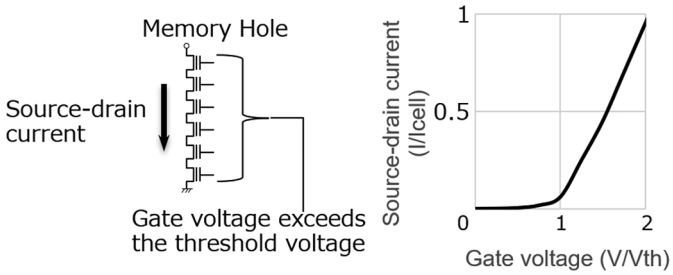

Fig. 2 Gate voltage and source–drain current: (a) circuit diagram and (b) *I–V* characteristics.

cylinder that stores charge, in turn enclosing a silicon dioxide cylinder as the tunnel dielectric that surrounds a central rod of conducting polysilicon, which acts as the conducting channel. The gate electrode of word line is formed by a tungsten layer that wraps around the cylinder and acts as the cell's gate electrode. There are select gates on the top and bottom tungsten layer.

1.2 Gate Voltage and Source–Drain Current

Analysis of source–drain current and threshold voltage is required to identify device failure mode in multilevel cell of memory structure. Figure 2 shows threshold voltage of gate voltage and source–drain current of a memory hole. Memory cells in different vertical layers do not interfere each other, as the charges cannot move vertically through the silicon nitride storage medium, and the electric fields associated with the gates are closely confined within each layer. Source–drain current flows through the channel when gate voltage exceeds threshold voltage. Reliable measurement method of source–drain current and uniformity of threshold voltage in multilevel cells is needed to identify failure mode.

1.3 Inline Electrical Characterization Challenges by e-Beam Inspection

E-beam inspection is widely used for inline electrical characterization of memory devices. Figure 3 shows an inline characterization challenges by utilizing e-beam inspection. E-beam inspection tool analyzes the variations in the image contrast of the structure to detect short, open, and void defects at middle of production line.[3,4] Meanwhile, accurate measurement of threshold voltage and the source–drain current is required to characterize memory cell through multilayers

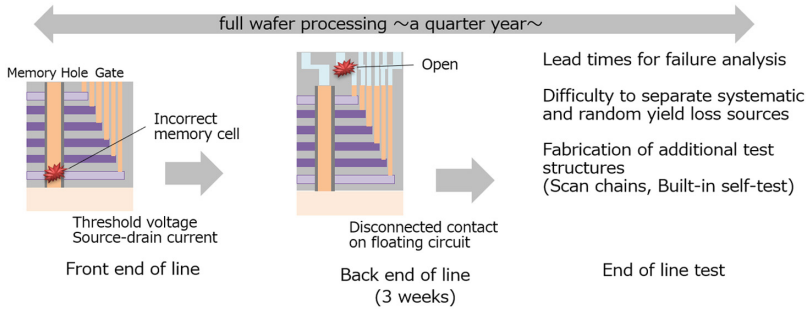

Fig. 3 Inline electrical characterization challenges.

as discussed in Sec. 1.2. However, in the subthreshold region of memory cell, voltage contrast (VC) is weakened due to gate voltage stimulated by electron dose of e-beam scanning.

Although threshold voltage and source–drain current are determined in process of front end of line, disconnected contacts on floating circuit are built in back end of circuit. The disconnected contact via on the floating circuit cannot be detected by e-beam inspection. The contact via the floating circuit appears as a dark VC due to the accumulation of charge that occurs during the precharging electron scanning. Similarly, the disconnected contact via on the floating circuit at a defect also appears as a dark VC.

The end of line test confounds systematic and random yield loss sources, thereby making it difficult to assess the impact of a specific (nonrandom) yield issue. Furthermore, additional testability features must be fabricated to perform physical probing such as scan chains or a "built-in self-test." Therefore, we developed inline solution of electrical property quantification method by a modulated electron microscopy.

2 Modulated Electron Microscopy

2.1 Voltage Contrast Enhancement by Modulated Electron Microscopy

VC of conventional e-beam scanning is not sufficient to identify defect mode in the subthreshold region of memory cell. The irradiation time dependence of VC is shown as Fig. 4. Red curve is VC of subthreshold region of memory cell, green curve closed gate of memory cell, blue curve contact on a floating circuit, and black curve disconnected contact. Contrast difference between the contact and the disconnected contact is reduced due to conductive path of a memory hole in case of conventional e-beam scanning. Moreover, optimization of scan rate and beam current could be expected to maximize VC, but determination of the beam scanning setting requires extensive evaluation lead time.

Figure 5 shows VC by the modulated beam scanning. The modulated beam scanning repeatedly cycles charging and discharging of the device circuit.[5] Existence of microcurrent leakage can be detected by the difference of VC images not only between the contact and the disconnected contact but also in the subthreshold region of memory cell.

Figure 6 shows memory hole images with conventional e-beam and modulated beam scanning. As for the experimental conditions, beam-acceleration voltage is 500 V, beam current is 500 pA, scan speed is TV and beam modulation period is sub-microsecond. The schematic in

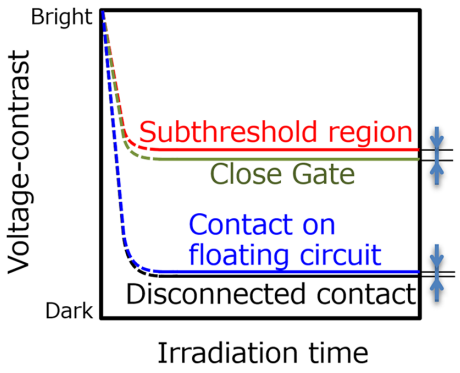

Fig. 4 Time dependence of VC in conventional e-beam.

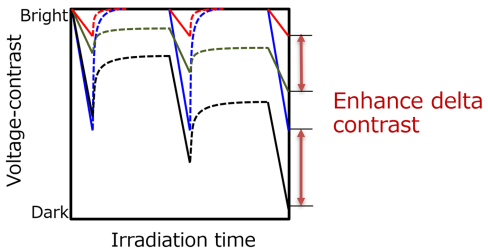

Fig. 5 Time dependence of VC in modulated beam scanning.

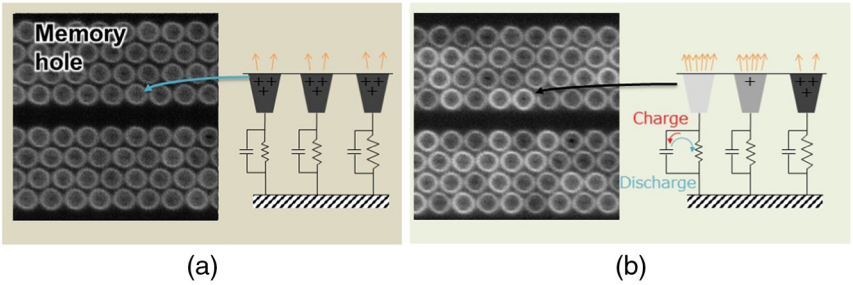

Fig. 6 Memory hole images: (a) conventional e-beam and (b) modulated electron microscope.

Fig. 6(a) is a memory hole image with conventional e-beam. Resistance between memory plug and ground affects charging of the plugs under e-beam irradiation. However, conventional e-beam scanning with continuous normalizes the amount of the plug charge, and VC in an e-beam image is not sufficient to identify the low resistance plug. Optimization of scan rate and beam current could maximize VC but determination of the beam scanning setting requires extensive evaluation lead time. The schematic in Fig. 6(b) is a memory hole image with modulated electron microscopy. The modulation beam scanning repeatedly charges and discharges circuits. Time constant difference between memory holes can be utilized to enhance VC by a modulated beam scanning.

2.2 Validation by Scanning Probe Microscopy

The modulated electron microscopy was validated by scanning probe microscopy as shown in Fig. 7. SEM was operated with accelerating voltage of 500 V, probe current of 500 pA, and field of view of 2 μm. The modulated electron microscopy shows deference of VC on channels of memory cell as shown in the schematic in Fig. 7(b). The test wafer was diced into test coupons after the modulated electron microscopy and used for scanning probe microscopy. Scanning probe microscopy was performed with the settings of substrate vias of 3 V, diamond coated probe, conductive cantilever, and a contact mode for measuring the local conductivity of a sample. It allows direct measurement of source–drain current of memory holes.

VC of conventional and modulated electron microscopy is compared with source–drain current by the scanning probe microscopy as shown in Fig. 8. In this figure, the result of conventional and modulated electron microscopy are plotted in (a) and (b), respectively. VC of e-beam and modulation electron microscopy are extracted from memory cell images. Although no trends can be seen for the conventional electron microscopy, VC of the modulated electron microscopy shows clear increasing trend with source–drain current.

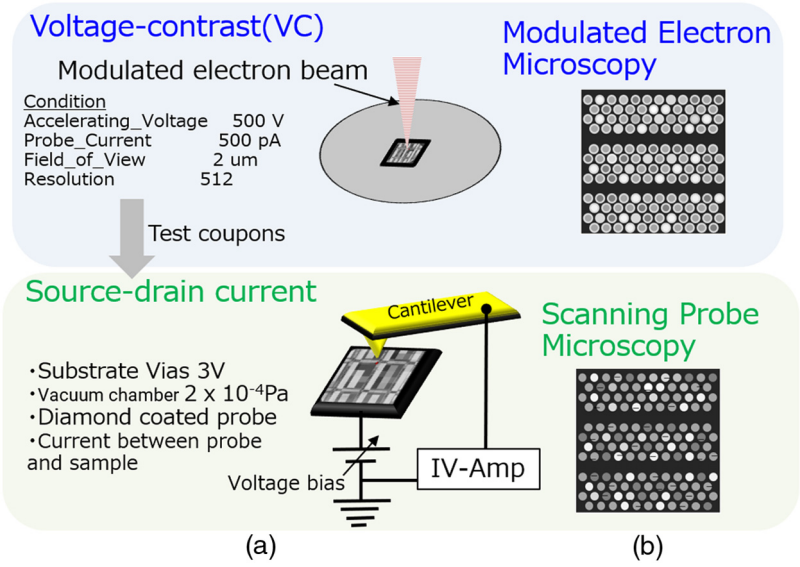

Fig. 7 (a) VC and (b) modulated electron microscopy and scanning probe microscopy.

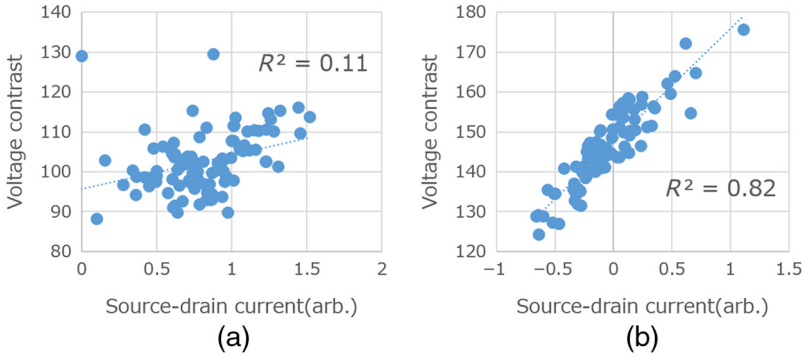

Fig. 8 Correlation between VC source–drain current obtained by (a) conventional e-beam and (b) the modulated electron microscopy.

By increasing the source–drain current in Fig. 8(b), VC of modulated electron microscopy is brighter, and the correlation coefficient (R^2) is 0.82 and the calibration curve has a direct relationship between two variables. Accordingly, the source–drain current estimated by VC of the modulated electron microscopy showed a positive correlation with scanning probe microscopy.

3 Validation in Full Wafer Process (Process Monitoring)

3.1 Measurement Method of Threshold Voltage

Measurement accuracy of threshold voltage of memory cells was confirmed for the modulated electron microscopy. As shown in the schematic of Fig. 9(a), electron beam was irradiated onto gates of memory cells, and VC of memory holes was captured.[6] The plot in the bottom of Figure 9(b) shows the dependence of opened memory hole ratio on charge by precharging electron scanning prior to image scanning.[7] Although dark VC appears on the memory hole after rapid electron scanning on the gates, the opened memory hole shows bright contrast by precharging. In the case where the opened memory hole rate is 50%, we define the precharging as accumulation of charge to identify the threshold voltage to conduct the source to drain terminals.

3.2 Inline Characterization of Memory Cell

Conventional electrical verification comprises full wafer processing and end of line test, and it typically takes four months. In addition, the end of line test is not able to assess the impact of a specific memory cell issue due to difficulty to separate systematic and random yield loss sources. If it is possible to detect defects and yield loss sources in a timely, device manufacturers might quickly identify and diagnose issues that arise during the manufacturing process. In this study,

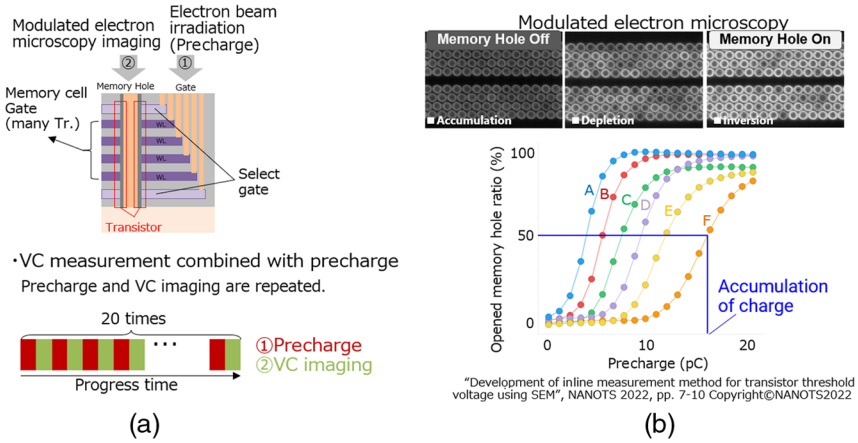

Fig. 9 Measurement method of threshold voltage: (a) cross section of sample and (b) precharge dependence of opened memory hole.

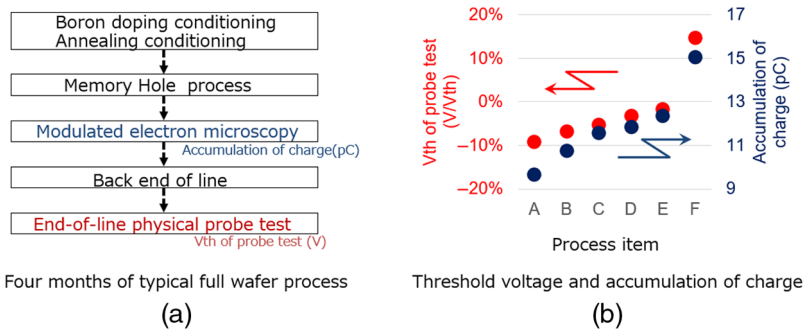

Fig. 10 Dependence of threshold voltage on process conditions: (a) 4 months full typical full wafer process and (b) threshold voltage and accumulation of charge.

the modulated beam microscopy was performed for memory samples with manipulating doping and annealing conditions in the middle of full wafer processing.

Figure 10(b) plots the dependence of threshold voltage on process conditions. Threshold voltage by the probe test is indicated with red mark, and the blue mark indicates accumulated charge obtained from by precharging versus gray level trend of modulated electron microscopy as defined in Sec. 3.1. By changing conditions of boron doping and annealing, threshold voltage by the physical probe test and the accumulated charge by the modulated electron microscopy shows the same trend for the different process conditions. This result implies strong correlation between the threshold voltage and the accumulated charge by the modulated electron microscopy.

3.3 Correlation with Physical Probe Test

We investigated the correlation of gate precharge for threshold voltage and source–drain current of memory cell. Threshold voltage and source–drain current were normalized by reference values, which are used as a benchmark for determining the quality of the manufacturing process. Figure 11 shows typical calibration curves measured by end of probe test. Figure 11(a) plots the dependence of the accumulation of charge on the threshold voltage. The threshold voltage is measurement result of physical probe method. The accumulation of charge shows clear correlation with the threshold voltage.

Figure 11(b) indicates the dependence of the accumulation of charge on the source–drain current. In the case of source–drain current, there is a linear relationship between two variables. Consequently, the threshold voltage and the source–drain current estimated by VC of the modulated electron microscopy showed good correlation with physical probe test.

3.4 Process Monitoring of Threshold Voltage and Source–Drain Current

An inline characterization to improve device development cycle is shown in Fig. 12. This is an example comparing conventional method and inline electrical characterization with enhancing VC by the modulated electron microscopy. Electrical characteristics cannot be measured by conventional method in the middle of manufacturing of integrated circuits. Furthermore, physical probe detects process variation after 4 weeks.

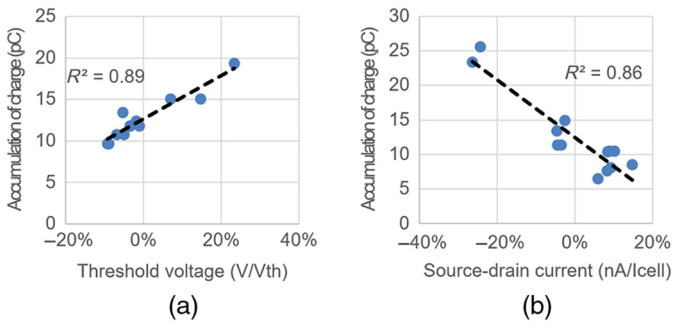

Fig. 11 (a), (b) Correlation with physical probe test.

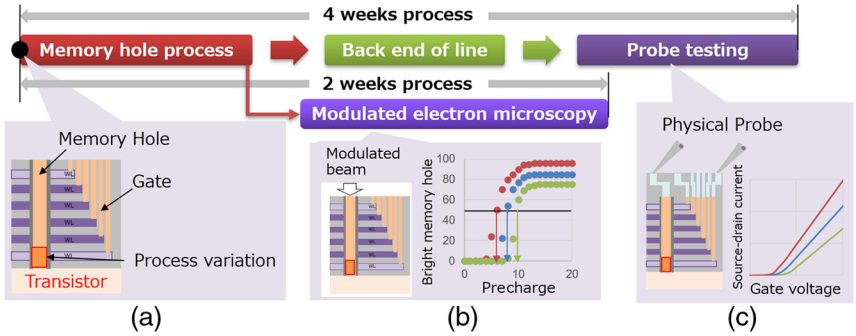

Fig. 12 Novel method of inline electrical characterization: (a) cross section image, (b) inline characterization, and (c) end of line probe test.

By utilizing the modulated electron microscopy, inline electrical characterization can be achieved before back end of line to detect and characterize yield loss issues 2 weeks earlier than conventional method. Moreover, this ability to detect and characterize memory cell issues inline is supposed to contribute to overcome bottleneck of the yield learning cycle. Accordingly, this inline electrical characterization is expected to reduce failure analysis lead time drastically and gain productivity improvement opportunities in the process. Additionally, the use of feedback and feedforward control method can help to further improve the fabrication of 3D NAND memory.

4 Validation in Full Wafer Process (Defect Inspection)

4.1 Defect Detection in Floating Circuit

In defect metrology for floating circuit as shown in Fig. 13, defects on floating circuits are mainly caused by particles, misalignment, incomplete etching, or improper filling. In the e-beam inspection, the contact via on the floating circuit appears as a dark VC due to the accumulation of charge that occurs during the precharging electron scanning. Similarly, the disconnected contact via on the floating circuit at a defect also appears as a dark VC. The accumulation of charge during the precharging electron scanning leads to the reduction of VC, which can make it difficult to accurately detect defects and variations in the device. Therefore, electrical characteristics cannot be measured by conventional method in the middle of chip manufacturing.

We applied the modulated electron microscopy for defect detection on full wafer process. As illustrated in the figure on the right bottom, VC can be enhanced using modulated electron microscopy. A contact via on floating circuit is bright VC and another contact via which is disconnected floating circuit is dark VC.

4.2 Comparison with Physical Probe Test

We have verified defect detection capability of the modulated electron microscopy for whole wafer region. As shown in Fig. 14(a), the modulated electron microscopy was carried out next to via process, and physical probe test was performed at end of the process line to verify the result of the modulated electron microscopy. The result of modulated electron microscopy and the physical probe test are shown in Fig. 14(b) and 14(c), respectively. In this figure, dark and bright via of the modulated electron microscopy are plotted in red and blue marks, respectively. Open

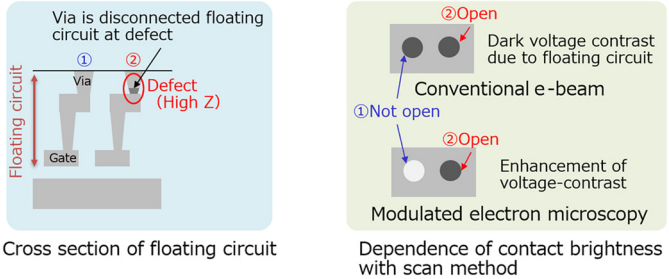

Fig. 13 Defect detection in floating circuit.

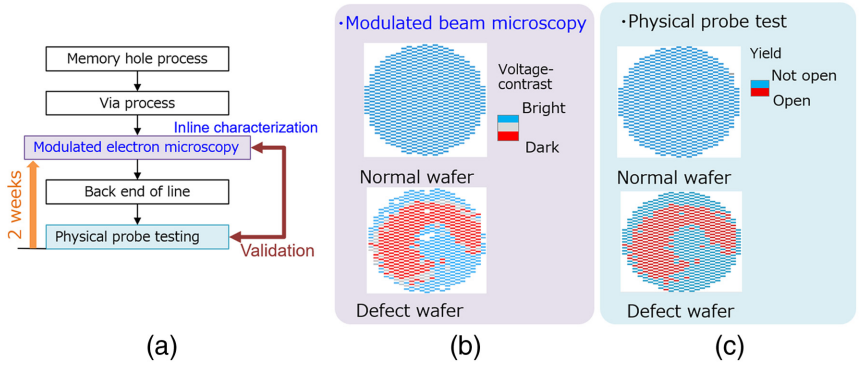

Fig. 14 Comparison of defect detection with physical probe test: (a) experimental flow, (b) modulated beam microscopy, and (c) mechanical probe method.

and not open via identified by the physical probe test are indicated in red and blue, respectively. The modulated electron microscopy detects wafer distribution of the dark vias. The dark vias distribution clearly reproduces the open vias over the whole wafer region. This result shows reliability of defect detection by the modulated electron microscopy.

This method can be faster than the conventional method that relies on physical probe testing, potentially leading to a reduction of 2 weeks in lead time. It could be due to a variety of factors such as process variations, material impurities, or design issues. Meanwhile, the wafer-wide inspection capability of inline electrical characterization enables clarification of systematic and random yield loss sources. By inline electrical characterization, it is possible to detect defects and yield loss sources in a timely. Accordingly, the modulated electron microscopy enables to keep high device yield with reducing the selling price of the working chips and to reduce the cost of wafer processing.

5 Conclusion

We developed the modulated electron microscopy with the SEM vector scan system to enhance VC and defect inspection capability. The modulated electron microscopy has been applied in the process monitoring of memory cell and the defect inspection of floating circuits.

Threshold voltage and source–drain current estimated by the method showed significant correlation with physical probe test. This can lead to the use of feedback and feedforward control method, which can help to further improve the fabrication of 3D NAND memory.

The modulated electron microscopy has overcome difficulty of open defect visualization in conventional electron scanning. The method also has been proved to be capable of wafer-wide open defect inspection by validating with physical probe test. The inline electrical characterization by the modulated electron microscopy before back end of line has ability to detect and characterize yield loss issues 2 weeks earlier than conventional method. Moreover, this ability supposes to contribute to overcome bottleneck of yield learning cycle.

The modulated electron microscopy is presently being applied in a SEM function named as VT-Scan of Hitachi review SEM CR7300. It is also important to continue evaluating and improving the technique to ensure its accuracy and efficiency and reliability. Logic and SRAM devices typically have smaller capacitance and resistance compared to memory devices, which often makes them unsuitable for modulated electron microscopy. This is because the smaller capacitance and resistance values result in a smaller time constant, which enables faster charging and discharging of the device circuit. As a result, the modulated VC signal can only be enhanced by increasing the frequency of the modulated beam scanning above the time constant of the device circuit.

Code, Data, and Materials Availability

The data utilized in this study were obtained from KIOXIA and Western Digital and Hitachi High-Tech. Data are available from the authors upon request, and with permission from KIOXIA and Western Digital and Hitachi High-Tech.

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References

1. H. Tanaka et al., "Bit cost scalable technology with punch and plug process for ultra-high density flash memory," in *Proc. IEEE Symp. VLSI Technol.*, pp. 14–15 (2007).
2. H. Aochi, "BiCS flash as a future 3D non-volatile memory technology for ultra-high density storage devices," in *Proc. IEEE Int. Memory Workshop*, May, pp. 1–2 (2009).
3. L. Reimer, *Scanning Electron Microscopy Physics of Image Formation and Microanalysis*, 2nd ed., pp. 299–308, Springer, Heidelberg (1998).
4. N. Tsuno et al., "Analysis of charging effects on highly resistive materials under electron irradiation by using transient-absorbed-current method," *J. Vac. Sci. Technol. B* **29**(3), 031209 (2011).
5. G. Yamazaki et al., "Yield improvement solution for semiconductor manufacturing to support increasing sophistication of digital society," *Hitachi Rev.* **71**(4), 66–71 (2022).
6. K. Nojima et al., "Development of in-line measurement method for transistor threshold voltage using SEM," in *NANOTS*, pp. 7–10 (2022).
7. M. Fukuda et al., "In-situ electrical property quantification of memory devices by modulated electron microscopy," *Proc. SPIE* **12496**, 124961O (2023).
8. H.-Y. Chang et al., "Calculation of secondary electron emission yields from low-energy electron deposition in tungsten surfaces," *Appl. Surf. Sci.* **450**, 190–199 (2017).

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